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ANNA UNIVERSITY

2013 REGULATION

**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

**EC6211- CIRCUITS AND DEVICES LAB**

(First Year B.E II Semester - Batch 2013)

LAB MANUAL

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**SYLLABUS**

**EC 6211 CIRCUITS AND DEVICES LABORATORY L T P C0 0 3 2**

**SYLLABUS**

|  |  |
| --- | --- |
| 1 | Characteristics of PN Junction Diode |
| 2 | Zener diode Characteristics & Regulator using Zener diode |
| 3 | Common Emitter input-output Characteristics |
| 4 | Common Base input-output Characteristics |
| 5 | FET Characteristics |
| 6 | SCR Characteristics |
| 7 | Clipper and Clamper & FWR |
| 8 | Verifications of Thevinin& Norton theorem |
| 9 | Verifications of KVL & KCL |
| 10 | Verifications of Super Position Theorem |
| 11 | Verifications of maximum power transfer & reciprocity theorem |
| 12 | Determination of Resonance Frequency of Series & Parallel RLC Circuits |
| 13 | Transient analysis of RL and RC circuits |

**TOTAL: 45 PERIODS**

**LIST OF EXPERIMENTS**

|  |  |  |
| --- | --- | --- |
| **EXPT NO.** | **NAME OF THE EXPERIMENT** | **PAGE NO.** |
| **CYCLE 1** | | |
| 1 | **Forward and Reverse Bias characteristics of PN junction diode and Zener diode.**   * **(a) Characteristics of PN junction diode** - The current values are measured for the applied voltages across the pn diode in forward and reverse bias condition and the graph is drawn. The forward and reverse bias resistance is calculated. * **(b) Characteristics of Zener diode-**- The current values are measured for the applied voltages across the zener diode in forward and reverse bias condition and the graph is drawn. The forward and reverse bias resistance is calculated. |  |
| 2 | **Characteristics of Transistor in common emitter configuration.**   * **Input characteristics**- The graph is plotted between input base-emitter voltage and the output base current for different values of collector-emitter voltage. * **Output Characteristics**- The graph is plotted between input collector-emitter voltage and the output collector current for different values of base current. |  |
| 3 | **Characteristics of Transistor in Common base configuration.**   * **Input characteristics**- The graph is plotted between input base-collector voltage and the output collector current for different value of collector-base voltage. * **Output Characteristics**- The graph is plotted between input collector-emitter voltage and the output collector current for different value of emitter current. |  |
| 4 | **Characteristic of JFET**   * **(a)Characteristics of JFET-**The transfer characteristics of a Junction Field Effect Transistor (JFET) is drawn and the thetransconductance (gm), drain to source resistance (rd), amplification factor (µ) are calculated. * **(b)Characteristics of MOSFET-** The transfer characteristics of a n-channel depletion type Metal Oxide Semiconductor Junction Field Effect Transistor (MOSFET) is plotted. |  |
| 5 | **Characteristics of SCR**   * Anode current is noted down for the various anode to cathode voltage for the particular firing current. The graph is plotted for the forward and reverse bias condition. |  |
| 6 | **Full wave Rectifier**   * **Full wave Rectifier-** The rectified output voltage for with and without filter of FWR is measured and the ripple factor is calculated. |  |
| 7 | **Clipper and Clamper**   * **Clipper-** The clipped output voltage is measured for the designed clipper circuit. * **Clamper-** The clamped output voltage is measured for the designed clamper circuit. |  |
| **CYCLE 2** | | |
| 8 | **Verification of Kirchhoff's circuit laws**   * **(a)KVL**-To prove KVL, voltage drop across each resistor is observed and sum of its value should be equal to the applied voltage of the loop for the given circuit. The values are compared with the theoretical value. * **(b)KCL**- For the given circuit the sum of values of the current at a particular node should be equal. The values are compared with the theoretical value. |  |
| 9 | **Verifications Of Thevenin’s& Norton theorem**   * **(a) Thevenin Theorems-** The theoretical and practical load current for the particular circuit which has the measured Thevein voltage series with Thevenin resistance is observed. * **(b) Norton’s Theorems**- The short circuited current parallel with the resistance is observed for the given circuit and the load current is measured. |  |
| 10 | **Verifications Of Super Position Theorem**   * The current for the particular branch of the given circuit due to each individual source is measured and its sum is equal to the total current. |  |
| 11 | **Verifications of maximum power transfer & reciprocity theorem**   * **(a) Maximum Power Transfer Theorem**- The power for different value of resistors for the given circuit is observed and to find out the resistor for which maximum power is transferred. * **(b) Reciprocity Theorem-**The current value for the circuit is measured before and after interchanging the voltage source from one branch to another. |  |
| 12 | **Determination Of Resonance Frequency of Series & Parallel RLC Circuits**   * **Frequency response of series RLC circuits** -The output voltage is measured for various frequencies for the series RLC circuit and the current value is calculated. The resonance frequency is obtained from the graph which has the maximum current value. * **Frequency response of parallel RLC circuits** - The output voltage is measured for various frequencies for the parallel RLC circuit and the current value is calculated. The resonance frequency is obtained from the graph which has the minimum current value |  |
| 13 | **Transient analysis of RL and RC circuits**   * The transient analysis is done by measuring the initial and final voltages across the capacitor and inductor and the time constant is also calculated. |  |
| **ADDITIONAL EXPERIMENTS** | | |
| **14** | **Characteristics of DIAC**   * The V-I characteristics of DIAC in both forward bias condition and reverse bias condition is analysed and plotted. |  |
| **15** | **Characteristics of TRIAC**   * The V-I characteristics of TRIAC in both forward bias condition and reverse bias condition is analysed and plotted. |  |
| **16** | **Characteristics of UJT**   * The characteristics of uni junction transistor (UJT) is analysed and the parameters like peak voltage (VP), valley point voltage (VV), valley point current (IV) and intrinsic standoff ratio (η) are determined from the plot. |  |
| **17** | **Characteristics of Photo Diode**   * The V-I characteristics of Photo Diode is analysed and plotted. |  |
|  | **DATA SHEETS** |  |

|  |  |
| --- | --- |
| **EXP NO: 1** | **FORWARD & REVERSE BIAS CHARACTERISTICS OF PN JUNCTION DIODE**  **AND ZENER DIODE** |
| **DATE:** |

1. **CHARACTERISTICS OF PN JUNCTION DIODE**

**AIM**

To study the forward and reverse bias characteristics of PN junction diode and hence to calculate forward and reverse resistance.

**COMPONENTS/EQUIPMENTS REQUIRED**

|  |  |  |  |
| --- | --- | --- | --- |
| **S.NO** | **COMPONENTS/EQUIPMENTS** | **RANGE** | **QUANTITY** |
| 1 | Regulated Power Supply | (0-30)V | 1 |
| 2 | Resistor | 1KΩ | 1 |
| 3 | DC Voltmeters | (0-1)V, (0-30)V | 1 |
| 4 | DC Ammeters | (0-100)mA,(0-100)µA, | 1 |
| 5 | Diode | 1N4007 | 1 |
| 6 | Bread board | - | 1 |
| 7 | Connecting wires | - | Few |

**THEORY:**

A semiconductor diode's current–voltage characteristic, or I–V curve, is related to the transport of carriers through the so-called depletion layer or depletion region that exists at the p-n junction between differing semiconductors.

If an external voltage is placed across the diode, an increasing electric field develops through the depletion zone which acts to slow and then finally stop recombination. At this point, there is a "built-in" potential across the depletion zone.

If an external voltage across the diode with the same polarity as the built-in potential, the depletion zone continues to act as an insulator, preventing any significant electric current flow. This is the reverse bias phenomenon.

However, if the polarity of the external voltage opposes the built-in potential, recombination can once again proceed, resulting in substantial electric current through the p-n junction. For silicon diodes, the built-in potential is approximately 0.6 V. Thus, if an external current is passed through the diode, about 0.6 V will be developed across the diode such that the P-doped region is positive with respect to the N-doped region and the diode is said to be "turned on" as it has a forward bias.

At very large reverse bias, beyond the peak inverse voltage or PIV, a process called reverse breakdown occurs which causes a large increase in current that usually damages the device permanently. Also, following the end of forward conduction in any diode, there is reverse current for a short time. The device does not attain its full blocking capability until the reverse current ceases.

The second region, at reverse biases more positive than the PIV, has only a very small reverse saturation current. The third region is forward but small bias, where only a small forward current is conducted.

As the potential difference is increased above an arbitrarily defined "cut-in voltage" or "on-voltage" or "diode forward voltage drop (Vd)", the diode current becomes appreciable, and the diode presents a very low resistance.

The current–voltage curve is exponential. In a normal silicon diode at rated currents, the arbitrary "cut-in" voltage is defined as 0.6 to 0.7 volts. The value is different for other diode types — Schottky diodes can be as low as 0.2 V and red light-emitting diodes (LEDs) can be 1.4 V or more and blue LEDs can be up to 4.0 V.

At higher currents the forward voltage drop of the diode increases. A drop of 1 V to 1.5 V is typical at full rated current for power diodes.

V-I Characteristic equation or diode current equation is,



Where, 

V = Applied voltage

= Efficiency (1 for germanium diode;

2 for silicon diode)

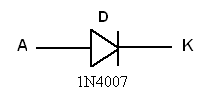
VT = voltage equivalent of temperature in volts

= kT volts

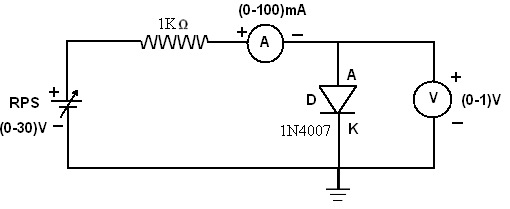
Where, k = Boltzmann’s constant = 8.62 X 10-5eV/0K

T = Temperature in 0K

**SYMBOL OF SEMICONDUCTOR DIODE:**



**FORWARD BIAS CHARACTERISTICS:**



**Circuit Diagram for Forward Bias**

**PROCEDURE:**

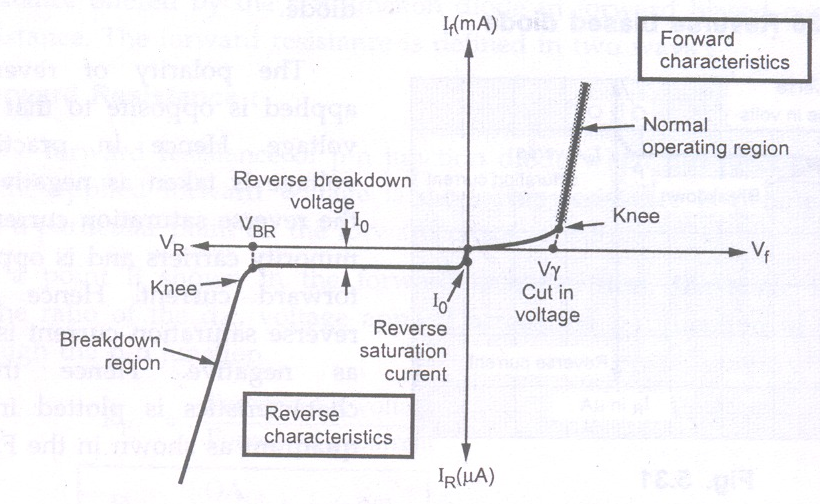
1. Connections are given as per the circuit diagram.
2. Power supply is switched ON.
3. By varying the Regulated Power Supply, the forward current is noted for various forward voltages.
4. The plot is drawn between the Forward voltage and Forward current.
5. From the plot the forward resistance is calculated.

**TABULATION**

**FORWARD BIAS**

|  |  |  |
| --- | --- | --- |
| **S.No** | **Forward Voltage**  **Vf (V)** | **Forward Current**  **If (mA)** |
| **1** |  |  |
| **2** |  |  |
| **3** |  |  |
| **4** |  |  |
| **5** |  |  |
| **6** |  |  |
| **7** |  |  |
| **8** |  |  |
| **9** |  |  |
| **10** |  |  |
| **11** |  |  |
| **12** |  |  |

**MODEL GRAPH:**

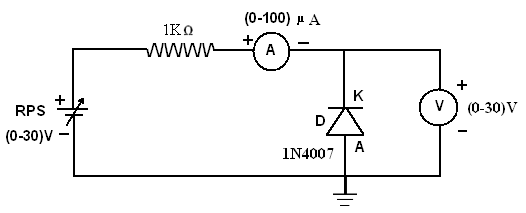
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**V-I Characteristics of a PN Diode**

**CALCULATION:**

Forward resistance, **rF=**

**REVERSE BIAS CHARACTERISTICS**

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**Circuit Diagram for Reverse Bias**

**PROCEDURE:**

1. Connections are given as per the circuit diagram.
2. Power supply is switched ON.
3. By varying the Regulated Power Supply, the reverse current is noted for various reverse voltages.
4. The plot is drawn between the reverse voltage and reverse current.
5. From the plot the reverse resistance is calculated.

**TABULATION**

**REVERSE BIAS**

|  |  |  |
| --- | --- | --- |
| **S.No** | **Reverse Voltage**  **Vr (V)** | **Reverse Current**  **Ir (µA)** |
| **1** |  |  |
| **2** |  |  |
| **3** |  |  |
| **4** |  |  |
| **5** |  |  |
| **6** |  |  |
| **7** |  |  |
| **8** |  |  |
| **9** |  |  |
| **10** |  |  |

**CALCULATION:**

1. Reverse resistance, 

**rr=**

**INFERENCE**

The characteristics of a PN junction diode is drawn and the forward and reverse dynamic resistances are

calculated as follows.

Forward resistance =

Reverse resistance =

Cut in voltage =

**REVIEW QUESTIONS**

1. What is Depletion region in a PN junction diode?
2. Explain the terms knee voltage and breakdown voltage
3. Define peak inverse voltage (PIV).
4. What is avalanche breakdown in PN junction diode?
5. List the applications of PN junction diode.
6. **CHARACTERISTICS OF ZENER DIODE**

**AIM**

To study the forward and reverse bias characteristics of Zener diode and to determine the reverse breakdown voltage, forward and reverse resistance.

**COMPONENTS/EQUIPMENTS REQUIRED**

|  |  |  |  |
| --- | --- | --- | --- |
| **S.NO** | **COMPONENTS/EQUIPMENTS** | **RANGE** | **QUANTITY** |
| 1 | Regulated Power Supply | (0-30)V | 1 |
| 2 | Resistor | 1KΩ | 1 |
| 3 | DC Voltmeter | (0-1)V | 1 |
| 4 | DC Ammeter | (0-100)mA | 1 |
| 5 | Zener Diode | IN4730 | 1 |
| 6 | Bread board | - | 1 |
| 7 | Connecting wires | - | Few |

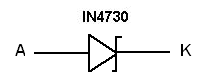
**THEORY:**

Zener diode is a special diode with increased amounts of doping. This is to compensate for the damage that occurs in the case of a *pn* junction diode when the reverse bias exceeds the breakdown voltage and thereby current increases at a rapid rate.

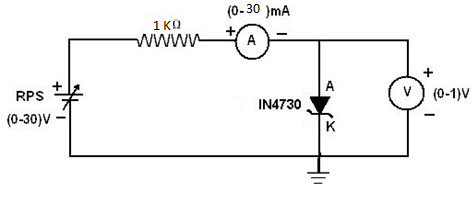
Applying a positive potential to the anode and a negative potential to the cathode of the zener diode establishes a forward bias condition. The forward characteristic of the zener diode is same as that of a *pn* junction diode i.e. as the applied potential increases the current increases exponentially. Applying a negative potential to the anode and positive potential to the cathode reverse biases the zener diode.

As the reverse bias increases the current increases rapidly in a direction opposite to that of the positive voltage region. Thus under reverse bias condition breakdown occurs. It occurs because there is a strong electric filed in the region of the junction that can disrupt the bonding forces within the atom and generate carriers. The breakdown voltage depends upon the amount of doping. For a heavily doped diode depletion layer will be thin and breakdown occurs at low reverse voltage and the breakdown voltage is sharp. Whereas a lightly doped diode has a higher breakdown voltage. This explains the zener diode characteristics in the reverse bias region.

**SYMBOL OF ZENER DIODE:**

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**FORWARD BIAS CHARACTERISTICS:**



**Circuit Diagram for Forward Bias**

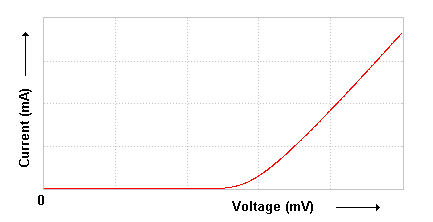
**PROCEDURE:**

1. Connections are given as per the circuit diagram.
2. Power supply is switched ON.
3. By varying the RPS, the forward current is noted for various forward voltages.
4. The plot is drawn between the Forward voltage and Forward current.
5. From the plot the forward resistance is calculated.

**TABLE FOR FORWARD BIAS:**

|  |  |  |
| --- | --- | --- |
| **S.No** | **Forward Voltage**  **Vf (V)** | **Forward Current**  **If (mA)** |
| **1** |  |  |
| **2** |  |  |
| **3** |  |  |
| **4** |  |  |
| **5** |  |  |
| **6** |  |  |
| **7** |  |  |
| **8** |  |  |
| **9** |  |  |
| **10** |  |  |
| **11** |  |  |

**MODEL GRAPH:**

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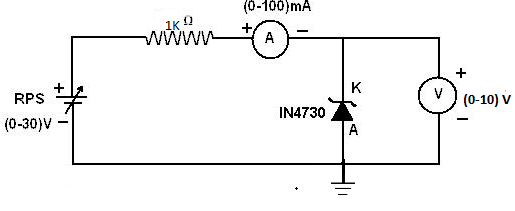
**Forward Characteristics of a Zener Diode**

**CALCULATION:**

Forward resistance, 

**rF=**

**REVERSE BIAS CHARACTERISTICS:**

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**Circuit Diagram for Reverse Bias**

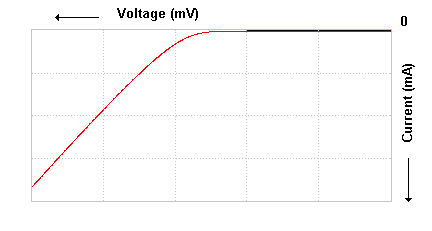
**PROCEDURE:**

1. Connections are given as per the circuit diagram.
2. Power supply is switched ON.
3. By varying the RPS, the reverse current is noted for various reverse voltages.
4. The plot is drawn between the reverse voltage and reverse current.
5. From the plot the reverse resistance is calculated.

**TABLE FOR REVERSE BIAS:**

|  |  |  |
| --- | --- | --- |
| **S.No** | **Reverse Voltage**  **Vr (V)** | **Reverse Current**  **Ir (mA)** |
| **1** |  |  |
| **2** |  |  |
| **3** |  |  |
| **4** |  |  |
| **5** |  |  |
| **6** |  |  |
| **7** |  |  |
| **8** |  |  |
| **9** |  |  |
| **10** |  |  |
| **11** |  |  |

**MODEL GRAPH:**

****

**Reverse Characteristics of a Zener Diode**

**CALCULATION:**

Reverse resistance, 

**rr=**

**INFERENCE**

The characteristics of a Zener diode is drawn.

Forward resistance =

Reverse resistance =

Reverse Breakdown voltage =

**REVIEW QUESTIONS**

1. List the applications of Zener Diode.
2. What is Zener Breakdown?
3. What is Avalanche breakdown?
4. What is the difference between a PN junction diode and a Zener diode?
5. How Zener diode acts as a regulator?

|  |  |
| --- | --- |
| **EXP NO: 2** | **CHARACTERISTICS OF TRANSISTOR IN COMMON EMITTER CONFIGURATION** |
| **DATE:** |

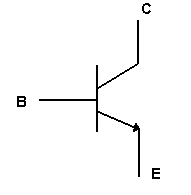
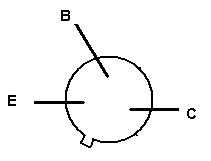
**AIM**

To study the input and output characteristics of given transistor in common emitter mode.

**COMPONENTS/EQUIPMENTS REQUIRED**

|  |  |  |  |
| --- | --- | --- | --- |
| **S.NO** | **COMPONENTS/EQUIPMENTS** | **RANGE** | **QUANTITY** |
| 1 | Regulated Power Supply | (0-30)V | 2 |
| 2 | Resistor | 1KΩ | 2 |
| 3 | DC Voltmeter | (0-30)V | 1 |
| 4 | DC Voltmeter | (0-10)V | 1 |
| 5 | DC Ammeter | (0-50)µA | 1 |
| 6 | DC Ammeter | (0-30)mA | 1 |
| 7 | BJT | BC107 | 1 |
| 8 | Bread board | - | 1 |
| 9 | Connecting wires | - | Few |

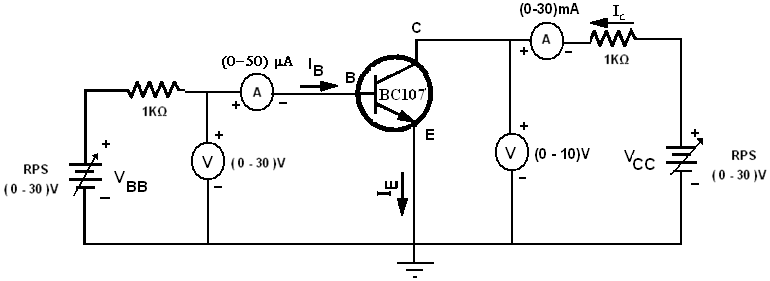
**THEORY:**



**Pin Diagram of BJT Symbol of BJT**

The input is applied between emitter and base and output is taken from the collector and emitter. Here, emitter of the transistor is common to both input and output circuits and hence the name common emitter (CE) configuration.

Regardless of circuit configuration, the base emitter junction is always forward biased while the collector-base junction is always reverse biased, to operate transistor in active region.

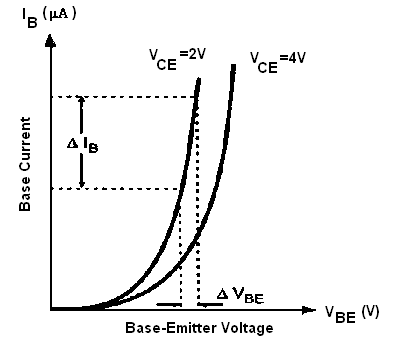


**Circuit Diagram for a BJT in CE Configuration**

**INPUT CHARACTERISTICS:**

**PROCEDURE:**

1. Connections are given as per the circuit diagram.
2. The supply is switched ON.
3. The collector-emitter voltage VCE is kept constant.
4. By varying the emitter-base voltage VBE, the various base current IB is noted.
5. The same procedure is repeated for various collector-emitter voltages VCE.
6. The input characteristic is the curve between input current IB and input voltage VBE at constant collector-emitter voltage VCE. The base current is taken along Y-axis and VBE along x-axis.



**Input Characteristics of a Transistor in CB Configuration**

**TABLE FOR INPUT CHARACTERISTICS:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| S.No | VCE = | | VCE = | |
| VBE(volts) | IB (µA) | VBE(volts) | IB (µA) |
| 1 |  |  |  |  |
| 2 |  |  |  |  |
| 3 |  |  |  |  |
| 4 |  |  |  |  |
| 5 |  |  |  |  |
| 6 |  |  |  |  |
| 7 |  |  |  |  |
| 8 |  |  |  |  |
| 9 |  |  |  |  |

**Calculation**

Input Resistance

Ri==

Ri**=**

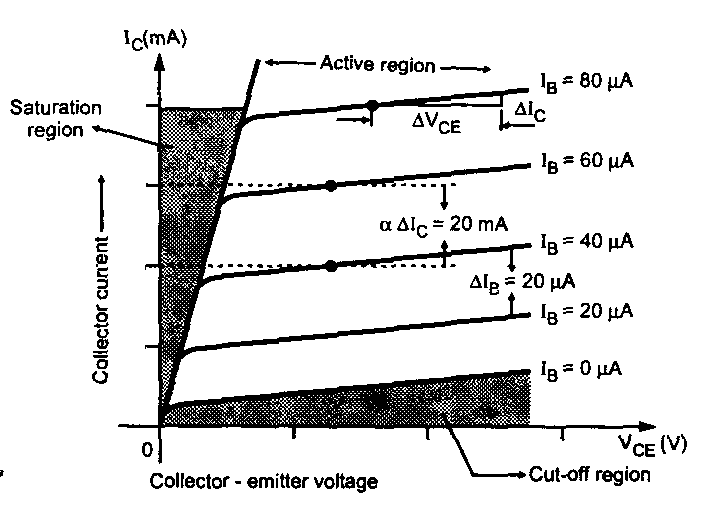
From this characteristic we observe the following important points.

1. As the input to a transistor in the CE configuration is between the base-to-emitter junctions, the CE input characteristics resembles a family of forward-biased diode curves.
2. After the cut-in voltage (barrier potential, normally 0.7 V for silicon and 0.3 V for Germanium), the base current (IB) increases rapidly with small increase in emitter-base voltage (VEB). It means that input resistance is very small. Because input resistance is a ratio of change in emitter-base voltage (∆VEB) to the resulting changes in base current (∆IB) at constant collector-emitter voltage (VCE), this resistance is also known as the dynamic input resistance of the transistor in CE configuration.
3. For a fixed value of VBE, IB decreases as VCE is increased. A larger value of VCE results in a large reverse bias at collector-base p-n junction. This increases the depletion region and reduces the effective width of the base. Hence, there are fewer recombinations in the base region, reducing the base current IB.

**OUTPUT CHARACTERISTICS:**

**PROCEDURE:**

1. Connections are given as per the circuit diagram.
2. The supply is switched ON.
3. The base current IBis kept constant.
4. By varying the collector-emitter voltage VCE, the various collector current IC is noted.
5. The same procedure is repeated for various base current IB.
6. The output characteristic is the curve between collector current IC and collector emitter voltage VCE at constant base current IB. The collector current is taken along Y-axis and collector-emitter voltage magnitude along X-axis.



**Output Characteristics of a Transistor in CB Configuration**

**TABLE FOR OUTPUT CHARACTERISTICS:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| S.No | IB = | | IB = | | IB = | |
| VCE(volts) | IC (mA) | VCE(volts) | IC (mA) | VCE(volts) | IC (mA) |
| 1 |  |  |  |  |  |  |
| 2 |  |  |  |  |  |  |
| 3 |  |  |  |  |  |  |
| 4 |  |  |  |  |  |  |
| 5 |  |  |  |  |  |  |
| 6 |  |  |  |  |  |  |
| 7 |  |  |  |  |  |  |
| 8 |  |  |  |  |  |  |
| 9 |  |  |  |  |  |  |
| 10 |  |  |  |  |  |  |

**Calculation**

Output Resistance

Ro==

Ro**=**

From the output characteristics we can see that,

1. The change in collector-emitter voltage (∆VCE) causes the little change in the collector current (∆IC) for constant base current IB.
2. The output characteristic of common emitter configuration consists of three regions: Active, Saturation, and cut-off.
3. **Active region**: The region where the curves are approximately horizontal is the “active” region of the CE configuration. In the active region, the collector junction is reverse biased. As VCE is increased, reverse bias increases. This causes depletion region to spread more in base than in collector, reducing the chances of recombination in the base.
4. **Saturation region** : If VCE is reduced to a small value such as 0.2 V, then collector-base junction becomes forward biased, since the emitter base junction is already forward biased by 0.7 V. The input junction in CE configuration is base to emitter junction, which is always forward biased to operate transistor in active region. Thus input characteristics of CE configuration are similar to forward characteristics of p-n junction diode. When both the junctions are forward biased, the transistor operates in the saturation region, which is indicated on the output characteristics. The saturation value of VCE, designated VCE (sat) usually ranges between 0.1 V to 0.3 V.
5. **Cut-off region**: When the input base current is made equal to zero, the collector current is the reverse leakage current. Accordingly, in order to cut-off the transistor, it is not enough to reduce IB = 0. Instead, it is necessary to reverse bias the emitter junction slightly. We shall define cut-off as the condition where the collector current is equal to reverse saturation current and the emitter current is zero.

**INFERENCE**

The input and output characteristics of transistor in CE mode is studied and plotted.

From graph, input resistance Ri=

Output resistance Ro =

|  |  |
| --- | --- |
| **EXP NO: 3** | **CHARACTERISTICS OF TRANSISTOR IN COMMON BASE CONFIGURATION** |
| **DATE:** |

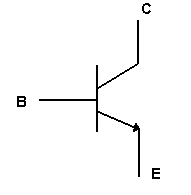
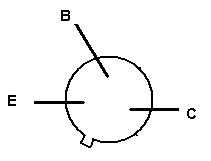
**AIM**

To study the input and output characteristics of given transistor in common base mode.

**COMPONENTS/EQUIPMENTS REQUIRED**

|  |  |  |  |
| --- | --- | --- | --- |
| **S.NO** | **COMPONENTS/EQUIPMENTS** | **RANGE** | **QUANTITY** |
| 1 | Regulated Power Supply | (0-30)V | 2 |
| 2 | Resistor | 1KΩ | 2 |
| 3 | DC Voltmeter | (0-30)V | 2 |
| 4 | DC Ammeter | (0-10)mA | 1 |
| 5 | DC Ammeter | (0-30)mA | 1 |
| 6 | BJT | BC107 | 1 |
| 7 | Bread board | - | 1 |
| 8 | Connecting wires | - | Few |

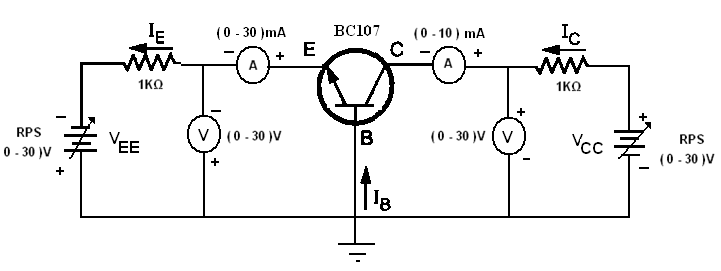
**THEORY:**



**Pin Diagram of BJT Symbol of BJT**

The input is applied between emitter and base and output is taken from the collector and base. Here, base of the transistor is common to both input and output circuits and hence the name common base configuration.

Regardless of circuit configuration, the base emitter junction is always forward biased while the collector-base junction is always reverse biased, to operate transistor in active region.

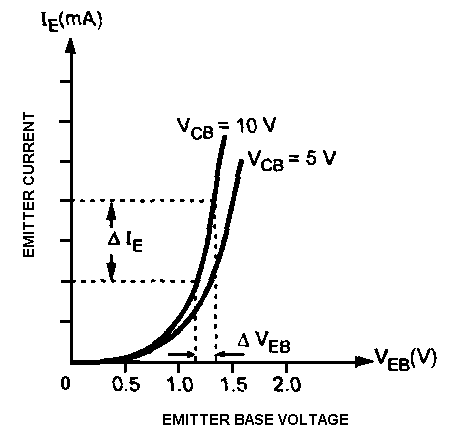


**Circuit Diagram for a BJT in CB Configuration**

**INPUT CHARACTERISTICS:**

**PROCEDURE:**

* 1. Connections are given as per the circuit diagram.
  2. The supply is switched ON.
  3. The collector-base voltage VCB is kept constant.
  4. By varying the emitter-base voltage VEB, the various emitter current IE is noted.
  5. The same procedure is repeated for various collector-base voltages VCB.
  6. The input characteristic is the curve between input current IE and input voltage VEB at constant collector-base voltage VCB. The emitter current is taken along Y-axis and emitter base voltage along X-axis.



**Input Characteristics of a Transistor in CB Configuration**

**TABLE FOR INPUT CHARACTERISTICS:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| S.No | VCB = 5V | | VCB = 10V | |
| VEB(volts) | IE (mA) | VEB(volts) | IE (mA) |
| 1 |  |  |  |  |
| 2 |  |  |  |  |
| 3 |  |  |  |  |
| 4 |  |  |  |  |
| 5 |  |  |  |  |
| 6 |  |  |  |  |
| 7 |  |  |  |  |
| 8 |  |  |  |  |
| 9 |  |  |  |  |

**Calculation**

Input Resistance

Ri==

Ri **=**

From this characteristic we can observe the following important points:

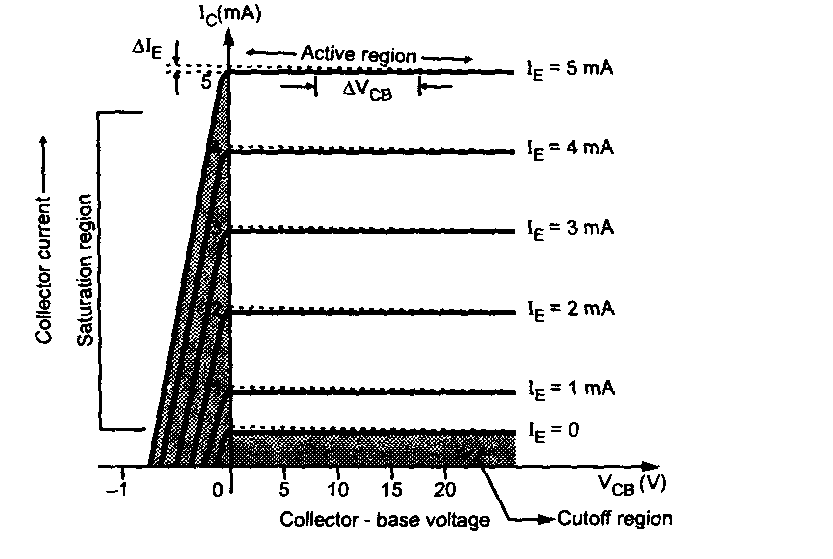
1. After the cut-in voltage (barrier potential, normally 0.7 V for silicon and 0.3 V for Germanium), the emitter current (IE) increases rapidly with small increase in emitter-base voltage (VEB). It means that input resistance is very small. Because input resistance is a ratio of change in emitter-base voltage (∆VEB) to the resulting changes in emitter current (∆IE) at constant collector-base voltage (VCB), this resistance is also known as the dynamic input resistance of the transistor in CB configuration.

2. It can be observed that there is slight increase in emitter current (IE) with increase in VCB. This is due to change in the width of the depletion region in the base region under the reverse biased condition.

**OUTPUT CHARACTERISTICS:**

**PROCEDURE:**

* 1. Connections are given as per the circuit diagram.
  2. The supply is switched ON.
  3. The emitter current IEis kept constant.
  4. By varying the collector-base voltage VCB, the various collector current IC is noted.
  5. The same procedure is repeated for various emitter current IE.
  6. The output characteristic is the curve between collector current IC and collector base voltage VCB at constant emitter current IE. The collector current is taken along Y-axis and collector-base voltage magnitude along X-axis.



**Output Characteristics of a Transistor in CB Configuration**

**TABLE FOR OUTPUT CHARACTERISTICS:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| S.No | IE = 0 mA | | IE = 2 mA | | IE = 4 mA | |
| VBC(volts) | IC (mA) | VBC(volts) | IC (mA) | VBC(volts) | IC (mA) |
| 1 |  |  |  |  |  |  |
| 2 |  |  |  |  |  |  |
| 3 |  |  |  |  |  |  |
| 4 |  |  |  |  |  |  |
| 5 |  |  |  |  |  |  |
| 6 |  |  |  |  |  |  |
| 7 |  |  |  |  |  |  |

**Calculation**

Output Resistance

Ro==

Ro **=**

From this characteristics we observe following points

1. The output characteristic has three basic regions: Active, cut-off and saturation.

|  |  |  |
| --- | --- | --- |
| State | Emitter Base Junction | Collector Base Junction |
| Active | Forward Biased | Reverse Biased |
| Cut-off | Reverse Biased | Reverse Biased |
| Saturation | Forward Biased | Forward Biased |

1. In active region, IC is approximately equal to IE and transistor works as an amplifier.
2. The region below the curve IE = 0 is called as cut-off region.
3. The saturation region is that region of the characteristics which is to the left of VCB =0 V. The exponential increase in collector current as the voltage VCB increases towards 0 V.
4. As IE increases IC also increases. Thus, IC depends upon input current IE but not on collector voltage. Hence, input current controls output current. Since transistor requires some current to drive it, it is called current operating device.

**INFERENCE**

The input and output characteristics of transistor in CB mode is studied and graph is plotted.

From the graph, Input resistance Ri = Output resistance R0 =

**REVIEW QUESTIONS**

1. What is a transistor?
2. What are the different configurations?
3. What are the parameters of transistor?
4. Is there any phase change between I/P and O/P voltages?
5. What are the hybrid parameters of a transistor?

|  |  |
| --- | --- |
| **EXP NO: 4** | **CHARACTERISTICS OF FIELD EFFECT TRANSISTOR** |
| **DATE:** |

**(a)CHARACTERISTICS OF JUNCTION FIELD EFFECT TRANSISTOR**

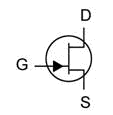
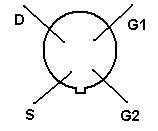
**AIM**

To plot the drain and transfer characteristics of a Junction Field Effect Transistor (JFET) and to calculate the transconductance (gm), drain to source resistance (rd), amplification factor (µ).

**COMPONENTS /EQUIPMENTS REQUIRED**

|  |  |  |  |
| --- | --- | --- | --- |
| **S.NO** | **COMPONENTS/EQUIPMENTS** | **RANGE** | **QUANTITY** |
| 1 | Regulated Power Supply | (0-30)V | 2 |
| 2 | Resistor | 220Ω | 2 |
| 3 | DC Voltmeter | (0-10)V | 1 |
| 4 | DC Voltmeter | (0-30)V | 1 |
| 5 | DC Ammeter | (0-30)mA | 1 |
| 6 | JFET | BFW11 | 1 |
| 7 | Bread board | - | 1 |
| 8 | Connecting wires | - | Few |

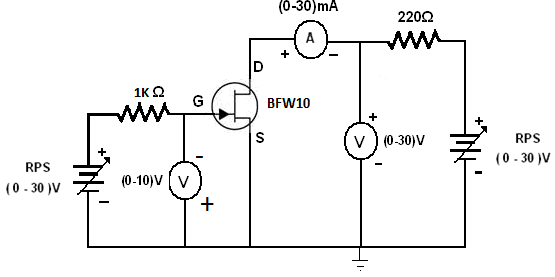
**THEORY:**

**N-channel JFET Pin Diagram**

The JFET is a long channel of semiconductor material, doped to contain abundance of positive charge carriers (*p-type*), or of negative carriers (*n-type*). Contacts at each end form the source and drain. The gate (control) terminal has doping opposite to that of the channel, which it surrounds, so that there is a P-N junction at the interface. Terminals to connect with the outside are usually made Ohmic .

The flow of electric charge through a JFET is controlled by constricting the current-carrying channel. The current depends also on the electric field between source and drain.



**Circuit Diagram for JFET**

**DRAIN CHARACTERICTICS:**

**PROCEDURE:**

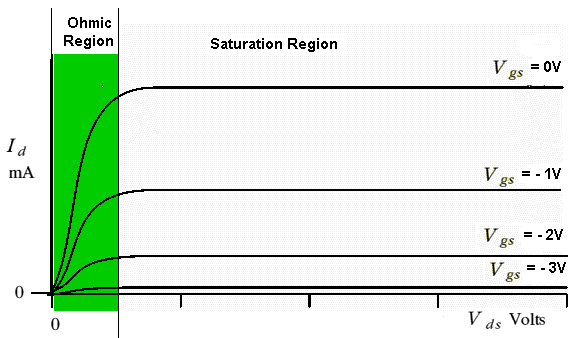
1. Connections are given as per the circuit diagram.

2. The supply is switched ON.

3. The gate-source voltage VGS is kept constant.

4. By varying the drain-source voltage VDS, the various drain current ID is noted.

5. The same procedure is repeated for various gate-source voltages (VGS)



In the Ohmic region, the drain-source voltage is small and the channel behaves like a fairly ordinary conductor. In this region the current varies roughly in proportion to the drain-source voltage as if the JFET obeys [*Ohm's law*](http://www.st-andrews.ac.uk/~www_pa/Scots_Guide/info/comp/passive/resistor/ohms_law/ohms_law.htm). However, as we increase the drain-source voltage and move into the region with a light background we increase the drain-channel voltage so much that we start to ‘squeeze down’ the channel.

**TABLE FOR DRAIN CHARACTERISTICS:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **S.No** | **VGS = 0.5V** | | **VGS = 1V** | |
| **ID (mA)** | **VDS(volts)** | **ID (mA)** | **VDS(volts)** |
| **1** |  |  |  |  |
| **2** |  |  |  |  |
| **3** |  |  |  |  |
| **4** |  |  |  |  |
| **5** |  |  |  |  |
| **6** |  |  |  |  |
| **7** |  |  |  |  |
| **8** |  |  |  |  |
| **9** |  |  |  |  |
| **10** |  |  |  |  |

**Calculation**

Drain Resistance

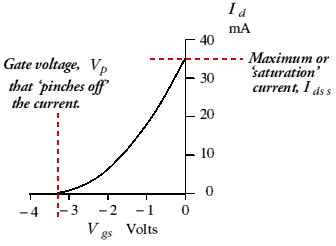
Rd==

RD **=**

**TRANSFER CHARACTERISTICS:**

**PROCEDURE:**

1. Connections are given as per the circuit diagram.
2. The supply is switched ON.
3. The drain-source voltage VDS is kept constant.
4. By varying the gate-source voltage VGS, the various drain current ID is noted.
5. The same procedure is repeated for various drain-source voltage VDS.



By looking at these curves we can see that the JFET has two areas of operation. At low (a few volts) drain-source voltages it behaves like a variable resistance whose value is controlled by the applied gate-source voltage. At higher drain-source voltages it passes a current whose value depends on the applied gate-source voltage. In most circuits it is used in this ‘high voltage’ region and acts as a voltage controlled current source.

JFET can be treated as a two port nonlinear network. The transfer characteristics wherein the input parameter is the voltage across gate and source, and the output parameter is the drain current are called the trans-conductance characteristics.

**TABLE FOR TRANSFER CHARACTERISTICS:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **S.No** | **VDS = 2V** | | **VDS = 4V** | |
| **VGS(volts)** | **ID (mA)** | **VGS(volts)** | **ID (mA)** |
| 1 |  |  |  |  |
| 2 |  |  |  |  |
| 3 |  |  |  |  |
| 4 |  |  |  |  |
| 5 |  |  |  |  |
| 6 |  |  |  |  |
| 7 |  |  |  |  |
| 8 |  |  |  |  |

Transconductance

gm==

**=**

**=**

gm**=**

**The transconductance is,**



**The drain to source resistance is,**



**The Amplification factor is,**

** =**

**INFERENCE**

The drain and transfer characteristics of the given JFET are determined and the parameters are calculated.

1. Drain Resistance =

2. Transconductance =

3. Amplification factor =

**REVIEW QUESTIONS**

1. Compare BJT and JFET
2. How is FET used as VVR?
3. What are the applications of FET?
4. What is meant by Gate -Source threshold voltage and pinch off voltage of JFET?
5. Differentiate JFET and MOSFET?

**(b)CHARACTERISTICS OF METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR (MOSFET)**

**AIM**

To plot the drain and transfer characteristics of a n-channel depletion type Metal Oxide Semiconductor Junction Field Effect Transistor (MOSFET).

**COMPONENTS & EQUIPMENTS REQUIRED:**

|  |  |  |  |
| --- | --- | --- | --- |
| **S.NO** | **COMPONENTS & EQUIPMENTS** | **RANGE** | **QUANTITY** |
| 1 | RPS | (0-30)V | 2 |
| 2 | Resistor | 220Ω | 2 |
| 3 | DC Voltmeter | (0-10)V | 1 |
| 4 | DC Voltmeter | (0-30)V | 1 |
| 5 | DC Ammeter | (0-30)mA | 1 |
| 6 | MOSFET |  | 1 |
| 7 | Bread board | - | 1 |
| 8 | Connecting wires | - | Few |

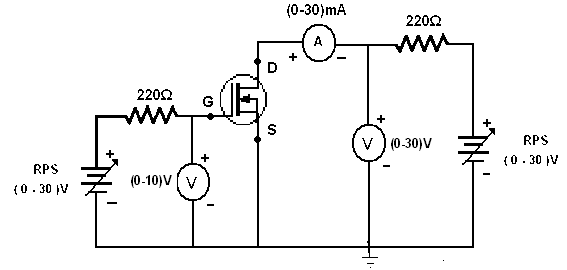
**THEORY**



**N-channel JFET**

The metal–oxide–semiconductor field-effect transistor (MOSFET, MOS-FET, or MOS FET) is a device used to amplify or switch electronic signals.

The MOSFET differs from JFET in that it has no p-n junction structure. Instead, the gate of the MOSFET insulated from the channel by a silicon dioxide (SiO2) layer. Due to this the input resistance of MOSFET is greater than JFET.

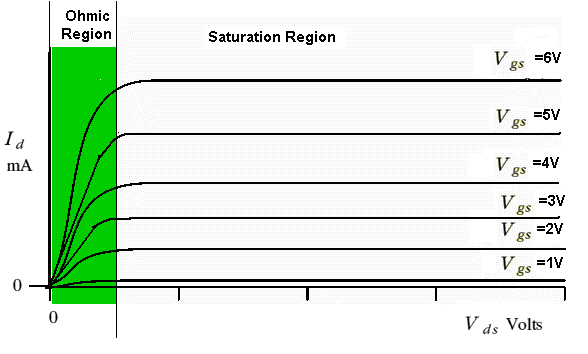
****

**Circuit Diagram for MOSFET**

**DRAIN CHARACTERICTICS**

**PROCEDURE**

1. Connections are given as per the circuit diagram.
2. The supply is switched ON.
3. The gate-source voltage VGS is kept constant.
4. By varying the drain-source voltage VDS, the various drain current ID is noted.
5. The same procedure is repeated for various gate-source voltage VGS.



In the Ohmic region, the drain-source voltage is small and the channel behaves like a fairly ordinary conductor. In this region the current varies roughly in proportion to the drain-source voltage as if the MOSJFET obeys [*Ohm's law*](http://www.st-andrews.ac.uk/~www_pa/Scots_Guide/info/comp/passive/resistor/ohms_law/ohms_law.htm). However, as we increase the drain-source voltage and move into the region with a light background we increase the drain-channel voltage so much that we start to ‘squeeze down’ the channel. It is similar to that of JFET only the difference is that it has positive part VGS.

**TABLE FOR DRAIN CHARACTERISTICS**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **S.No** | **VGS = 3V** | | **VGS = 3.2V** | |
| **ID (mA)** | **VDS(volts)** | **ID (mA)** | **VDS(volts)** |
| **1** |  |  |  |  |
| **2** |  |  |  |  |
| **3** |  |  |  |  |
| **4** |  |  |  |  |
| **5** |  |  |  |  |
| **6** |  |  |  |  |
| **7** |  |  |  |  |
| **8** |  |  |  |  |
| **9** |  |  |  |  |
| **10** |  |  |  |  |

Drain Resistance

Rd==

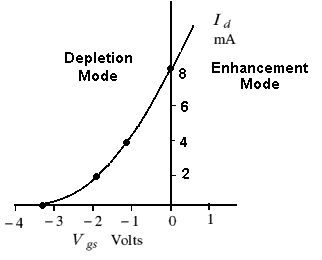
**=**

RD **=**

**TRANSFER CHARACTERISTICS:**

**PROCEDURE:**

1. Connections are given as per the circuit diagram.
2. The supply is switched ON.
3. The drain-source voltage VDS is kept constant.
4. By varying the gate-source voltage VGS, the various drain current ID is noted.
5. The same procedure is repeated for various drain-source voltage VDS.



For positive values of VGS the positive gate will draw additional electrons from the p-type substrate due to reverse leakage current and establish new carries through the collisions between accelerating particles. Because of this, as gate to source voltage increases in positive direction, the drain current also increases.

**TABLE FOR TRANSFER CHARACTERISTICS**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **S.No** | **VDS = 2 V** | | **VDS = 4 V** | |
| **VGS(volts)** | **ID (mA)** | **VGS(volts)** | **ID (mA)** |
| 1 |  |  |  |  |
| 2 |  |  |  |  |
| 3 |  |  |  |  |
| 4 |  |  |  |  |
| 5 |  |  |  |  |
| 6 |  |  |  |  |
| 7 |  |  |  |  |
| 8 |  |  |  |  |

Transconductance

gm==

**=**

gm **=**

**INFERENCE**

The drain and transfer characteristics of a metal oxide semiconductor junction field effect transistor is analyzed.

|  |  |
| --- | --- |
| **EXP NO: 5** | **CHARACTERISTICS OF SCR** |
| **DATE:** |

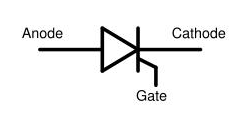
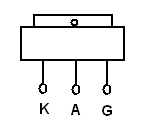
**AIM**

To study and plot the forward and reverse characteristics of silicon controlled rectifier (SCR).

**COMPONENTS /EQUIPMENTS REQUIRED**

|  |  |  |  |
| --- | --- | --- | --- |
| **S.NO** | **COMPONENTS/EQUIPMENTS** | **RANGE** | **QUANTITY** |
| 1 | Regulated Power Supply | (0-30)V | 2 |
| 2 | Resistor | 1KΩ | 2 |
| 3 | DC Voltmeter | (0-10)V | 1 |
| 4 | DC Ammeter | (0-30)mA | 2 |
| 5 | DC Ammeter | (0-3)mA | 1 |
| 6 | SCR | 2P4M | 1 |
| 7 | Bread board | - | 1 |
| 8 | Connecting wires | - | Few |

**THEORY:**



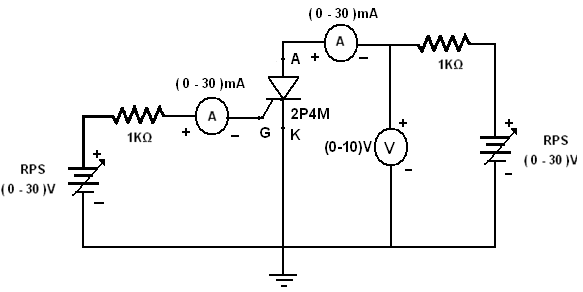
**Pin Diagram of SCR Symbol of SCR**

The SCR is a unidirectional device has two states, ON or OFF, and it allows current to flow in only one direction.

SCR's can remain in the OFF state even though the applied potential may be several thousand volts. In the ON state, they can pass several thousand amperes. When a small signal is applied between the gate and cathode terminals, the SCR will begin conducting within 3 microseconds. Once turned on, it will remain on until the current through it is reduced to a very low value, called the holding current.

Because the SCR allows current to flow in only one direction, two SCR's are connected in an inverse parallel configuration to control AC current.

**FORWARD CHARACTERISTICS:**



**PROCEDURE:**

1. Connections are given as per the circuit diagram.

2. The supply is switched ON.

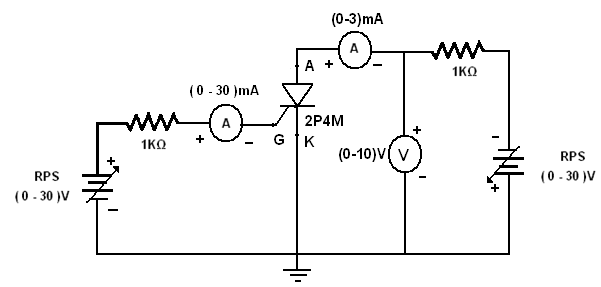
3. Set the gate current IG equal to firing current.

4. Vary the anode to cathode voltage (VAK) and note down the corresponding anode current IA. Note that the VAK suddenly drops and there is a sudden increase in the IA.

5. Repeat the above procedure for various gate current IG.

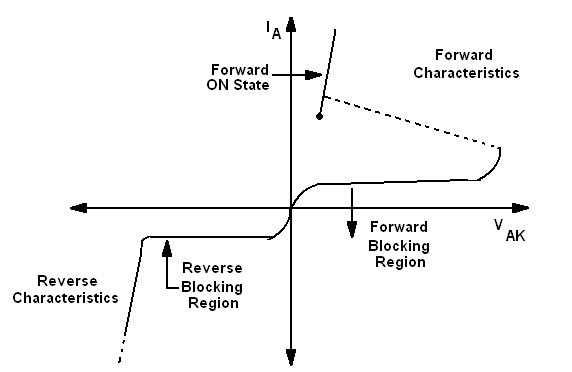
6. Plot the graph between VAK and IA.

**REVERSE CHARACTERISTICS:**



**PROCEDURE:**

1. Connections are given as per the circuit diagram.
2. The supply is switched ON.
3. Set the gate current IG equal to firing current.
4. Vary the anode to cathode voltage (VAK) and note down the corresponding anode current IA. Note that the IA is negligibly small and practically it is neglected.
5. Repeat the above procedure for various gate current IG.
6. Plot the graph between VAK and IA.



**Characteristics of a SCR**

**TABULATION**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **S.No** | **Forward Bias** | | **Reverse Bias** | |
| **IG­= 25mA** | | **IG­= 25mA** | |
| **VAK(volts)** | **IA (mA)** | **VAK(volts)** | **IA (mA)** |
| 1 |  |  |  |  |
| 2 |  |  |  |  |
| 3 |  |  |  |  |
| 4 |  |  |  |  |
| 5 |  |  |  |  |
| 6 |  |  |  |  |

**INFERENCE**

The forward and reverse characteristics of the SCR is studied and drawn.

**REVIEW QUESTIONS**

1. What is SCR?
2. Why SCR cannot be used as Bidirectional Switch?
3. Define Latching current.
4. Define Holding current.
5. Define Breakdown voltage and Breakover voltage.

|  |  |
| --- | --- |
| **EXP NO: 6** | **FULL WAVE RECTIFIER** |
| **DATE:** |

**Aim**

To construct a full wave rectifier and to measure dc voltage under load and to calculate the ripple factor.

**COMPONENTS /EQUIPMENTS REQUIRED**

|  |  |  |  |
| --- | --- | --- | --- |
| **S.NO.** | **COMPONENTS/EQUIPMENTS** | **RANGE** | **QUANTITY** |
| 1. | Transformer | 230 V / 6-0-(-6) | 1 |
| 2. | Diode | 1N4007 | 2 |
| 3. | Resistor | 1 kΩ | 1 |
| 4. | Capacitor | 100µf | 2 |
| 5 | Regulated power supply | (0-30)V | 1 |
| 6 | Signal Generator | (0-3)MHz | 1 |
| 7 | CRO | 30 MHz | 1 |
| 8 | Bread Board |  | 1 |
| 9 | Connecting Wires | Single strand | as reqd. |

**Theory**

The full wave rectifier conducts for both the positive and negative half cycles of the input ac supply. In order to rectify both the half cycles of the ac input, two diodes are used in this circuit. The diodes feed a common load RL with the help of a centre tapped transformer. The ac voltage is applied through a suitable power transformer with proper turn’s ratio. The rectifier’s dc output is obtained across the load. The dc load current for the full wave rectifier is twice that of the half wave rectifier. The lowest ripple factor is twice that of the full wave rectifier. The efficiency of full wave rectification is twice that of half wave rectification. The ripple factor also for the full wave rectifier is less compared to the half wave rectifier.

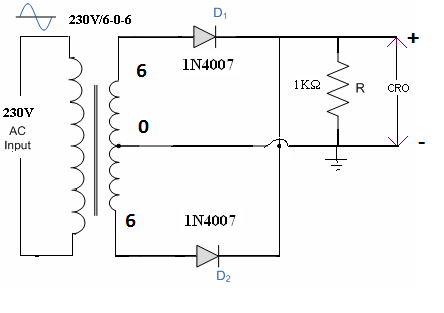
**Formula USED**

Ripple Factor = √ [(Vm/√2) / (2\*Vm /л)] 2-1

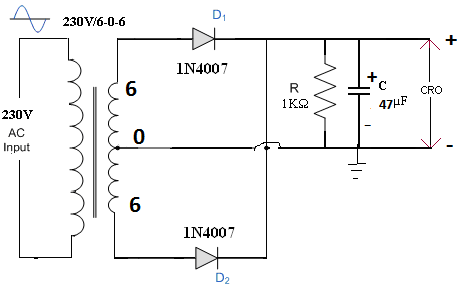
Where Im is the peak current

**CIRCUIT DIAGRAM**

**FULLWAVE RECTIFIER WITHOUT FILTER**



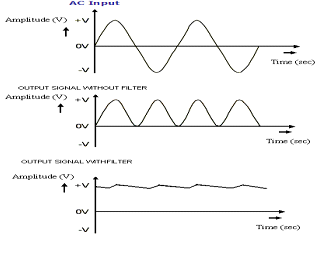
**FULLWAVE RECTIFIER WITH FILTER**



**Calculation**

* + - 1. D
      2. \*100

**MODEL GRAPH**



**TABULATION:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Input signal** | | **Output signal** | | | |
| **Without filter** | | **With filter** | |
| **Amplitude(V)** | **Time period**  **(ms)** | **Amplitude(V)** | **Time period**  **(ms)** | **Amplitude(V)** | **Time period (ms)** |
|  |  | 5 | TON1= |  | TC= |
| TON2= | TD= |

**Procedure:**

1. Connections are given as per the circuit diagram wiyhout filter.
2. Note the amplitude and time period of the input signal at the secondary winding of the transformer and rectified output.
3. Repeat the same steps with the filter and measure Vdc.
4. Calculate the ripple factor.
5. Draw the graph for voltage versus time.

**INFERENCE**

The full wave rectifier was constructed and its input and output waveforms are drawn. The ripple factor of capacitive filter is calculated as,

Ripple factor: i) With filter = ii) Without filter =

**REVIEW QUESTIONS**

1. What is a full wave rectifier?
2. What is the value of the ripple factor of a full wave rectifier?
3. What is the maximum efficiency that can be obtained in a full wave rectifier?
4. What is the advantage of full wave rectifier over half wave rectifier?
5. Define Transformer utilization factor.

|  |  |
| --- | --- |
| **EXP NO: 7** | **CLIPPERS AND CLAMPERS** |
| **DATE:** |

**AIM:**

To construct and test clippers and clampers circuit and to observe the output waveform.

**COMPONENTS /EQUIPMENTS REQUIRED**

|  |  |  |  |
| --- | --- | --- | --- |
| **S,NO** | **COMPONENTS/EQUIPMENTS** | **SPECIFICATION** | **QUANTITY** |
|  | Diode | 1N4007 | 2 |
|  | Resistor | 560Ω | 2 |
|  | Capacitor | 1µF | 2 |
|  | Function Generator | 0-3MHZ | 1 |
|  | Bread board, connecting wires. | - | 1,few |

**THEORY**

**CLIPPERS**

Clippers have the ability to clip off a portion of the input signal without distorting the remaining part of the alternating waveform.. The half wave recitifier is an example of the simplest form of diode clipper – one resistor and diode. Depending upon the orientation of the diode , the positive or negative region of the input signal is clipped off.

Clippers are of two : I . Series ii. Parallel

Series configuration is defined as one where diode is in series with the load, while the parallel the diode is connected in parallel to the load.

**CLAMPERS**

The clamping network is one that will clamp a signal to different dc level. The circuit has a diode, resistor and a capacitive element, but it can also employ an independent dc supply to introduce an additional shift. The magnitude of R and C must be chosen that the time constant τ = RC is large enough that the voltage across the capacitor does not discharge significantly during the interval diode is nonconducting.

**PROCEDURE**

(i)Connect the differentiator circuit. Adjust the signal generator to produce a 1V peak

a. sine wave at 100Hz.

b. square wave at 100 Hz

(ii) Observe i/p and o/p waveform on the oscilloscope .Measure and record the peak value of Vo and the phase angle of Vo w.r.t Vi.

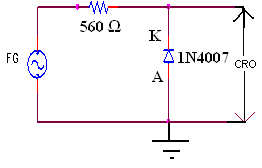
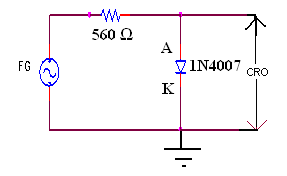
(iii) Connect the integrator circuit Adjust the signal generator to produce a 1V peak

a. sine wave at 5kHz. b. square wave at 5kHz

iv.Observe and record the input and the output waveforms.

**CLIPPERS**

POSITIVE CLIPPER NEGATIVE CLIPPER

****

**TABULATION**

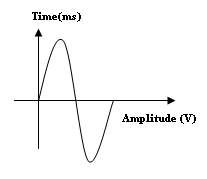
**POSITIVE CLIPPER NEGATIVE CLIPPER**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | **Amplitude**  **(in volts)** | **Time Period**  **(in msec)** |  |  | **Amplitude**  **(in volts)** | **Time Period**  **(in msec)** |
| **Input** |  |  | **Input** |  | **8** |
| **Output** |  |  | **Output** |  |  |

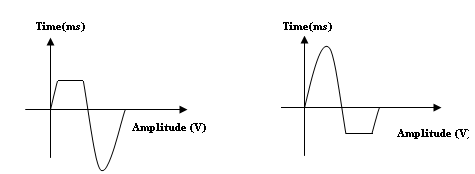
**MODEL GRAPH**

**CLIPPERS:**

**INPUT SIGNAL:**

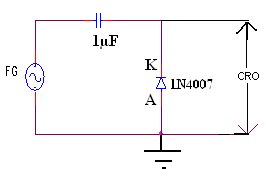
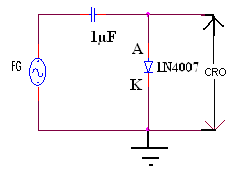
****

**POSITIVE CLIPPED OUTPUT: NEGATIVE CLIPPED OUTPUT:**

****

**CLAMPERS**

**POSITIVE CLAMPER NEGATIVE CLAMPER**

****

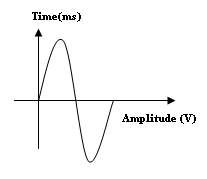
**TABULATION**

**POSITIVE CLAMPER NEGATIVE CLAMPER**

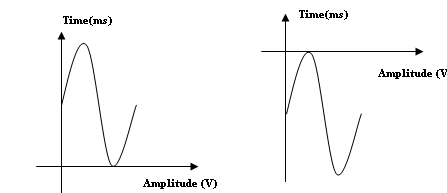
|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | **Amplitude**  **(in volts)** | **Period**  **(in sec)** |  |  | **Amplitude**  **(in volts)** | **Period**  **(in sec)** |
| **Input** |  |  | **Input** |  |  |
| **Output** |  |  | **Output** |  |  |

**CLAMPERS:**

**INPUT SIGNAL:**

****

**POSITIVE CLAMPED OUTPUT: NEGATIVE CLAMPED OUTPUT:**

****

**INFERENCE**

The Clipper and Clamper circuit was constructed and its input and output waveforms are drawn

**REVIEW QUESTIONS**

1.What are clippers and clampers?

2.Give some applications of clippers and clampers.

|  |  |
| --- | --- |
| **EXP NO: 8** | **VERIFICATION OF KIRCHHOFF’S LAWS**  **(**USING MESH AND NODAL ANALYSIS) |
| **DATE:** |

**AIM**

To verify Kirchhoff’s Voltage Law (KVL) &Kirchhoff’s Current Law (KCL) using mesh and nodal analysis of the given circuit.

**COMPONENTS/EQUIPMENTS REQUIRED**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **S.NO** | **COMPONENTS/EQUIPMENTS** | **TYPE** | **RANGE** | **QUANTITY** |
| 1 | Regulated Power Supply | DC | (0-30)V | 1 |
| 2 | Resistor | - | 1KΩ | 3 |
| 3 | Voltmeter | DC | (0-10)V | 3 |
| 4 | Bread board | - | - | 1 |
| 5 | Connecting wires | - | - | Few |

**THEORY**

Kirchhoff’s laws relate to the conservation of energy, which states that energy cannot be created or destroyed, only changed into different forms. This can be expanded to laws of conservation of voltage and current. In any circuit, the voltage across each series component (carrying the same current) can be added to find the total voltage. Similarly, the total current entering a junction in a circuit must equal the sum of current leaving the junction.

**(a)KIRCHHOFF’S CURRENT LAW "KCL"**

Kirchhoff’s ‘‘current law’’ is based upon the fact that at any connecting point in a network the sum of the currents flowing toward the point is equal to the sum of the currents flowing away from the point. The law is illustrated in the examples in Fig.(1), where the arrows show the directions in which it is given that the currents are flowing. (The number alongside each arrow is the amount of current associated with that arrow.)



***Fig.1***

|  |
| --- |
| The sum of the currents flowing **TO** a node point equals the sum of the currents flowing **FROM** that point. |

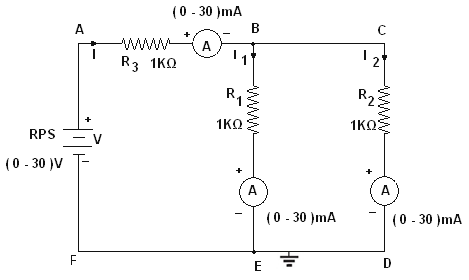
However, by Kirchhoff’s current law, **I3 = I1 + I2**, and thus, as shown in Fig. (1), we need to use only two current designations. In other words, if we know any two of the three currents, we can then find the third current. In the same way, if there are, say, four branch currents entering and leaving a node point, and if we know any three of the currents, we can then find the fourth current, and so on.

|  |
| --- |
| I1 + I2=I3  I1+I2-I3=0 |

The Kirchhoff’s current law can be state in the form:

|  |
| --- |
| **The algebraic sum of the currents at a node (junction point) is equal to zero.** |

**CIRCUIT DIAGRAM**

****

**THEORETICAL CALCULATION:**

**= 1K** **= 1K ;** **= 1K**





=1.5kΩ

**Let V = 5V,**



=3.3mA

I1= I\*R2 =1.65mA

R1+R2

I2= I\*R1

R1+R2

=1.65mA

**PROCEDURE:**

**KIRCHOFF’S CURRENT LAW:**

1. The circuit connections are given as per the circuit diagram.
2. Switch ON the power supply.
3. Initially set 5V as input voltage from RPS.
4. The ammeter readings are noted and the values are tabulated.
5. The same procedure is repeated for various values.

**TABULATION: Let V = 5V , So I = 3.3 mA**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | Resistance in Ohms | | | | Current in mA | | |
| R1 | R2 | R3 | RT | I1 | I2 | I = I1+I2 |
| Theoritical | 1KΩ | 1KΩ | 1KΩ | 1.5KΩ |  |  |  |
| Practical | 1KΩ | 1KΩ | 1KΩ | 1.5KΩ |  |  |  |

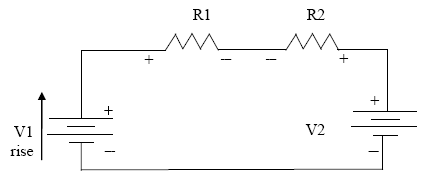
**(b)KIRCHHOFF’S VOLTAGE LAW "KVL"**

It states as follows:

|  |
| --- |
| ***The algebraic sum of the products of currents and resistance in each of the conductors in any closed path (or mesh) in a network plus the algebraic sum of the e.m.fs. in that path is zero.*** |

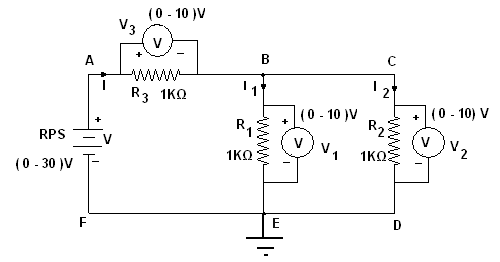
In other words, Σ *IR + Σ e.m.f. = 0 (*round a mesh)

Let us now write the equation for Fig. (2) in accordance with Kirchhoff’s voltage law. To do this, we start at any point, such as A, and move completely around the circuit (we will assume in the CW sense here), listing the ‘‘voltage drops’’ and the ‘‘voltage rises’’ as we go. (In doing this, remember that we have defined that going from ‘‘minus to plus’’ constitutes a **RISE** in voltage and going from ‘‘plus to minus’’ constitutes a **DROP** in voltage.) Thus, if we agree to list all ‘‘voltage drops’’ on the left-hand sides of our equations and all the ‘‘voltage rises’’ on the right-hand sides, the Kirchhoff voltage equation for Fig. (2) is***R1 I + V2 + R2 I = V1***



***Fig.2***

**CIRCUIT DIAGRAM**

****

**Circuit Diagram for Kirchoff’s Voltage Law**

**THEORETICAL CALCULATION:**

**= 1K** **= 1K ;** **= 1K**





=1.5KΩ

**Let V = 5V,**

=3.33mA

I1= I\*R2

R1+R2

=1.67mA

V1=I1\*R1=1.67V

V3=I\*R3=3.33V

**In the loop ABEFA,**

**= 5V**

**PROCEDURE:**

**KIRCHOFF’S VOLTAGE LAW:**

1. The circuit connections are given as per the circuit diagram.
2. Switch ON the power supply.
3. Initially set 5V as input voltage from RPS.
4. The voltmeter readings are noted and the values are tabulated.
5. The same procedure is repeated for various values.

**TABULATION:**

**Let V = 5V**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Resistance in Ohms | | | | Voltage in Volts | | | V = V1 + V3  = V2 + V3 (V) |
| R1 | R2 | R3 | RT | V1 | V2 | V3 |
| Theoretical | 1KΩ | 1KΩ | 1KΩ | 1.5KΩ |  |  |  |  |
| Practical | 1KΩ | 1KΩ | 1KΩ | 1.5KΩ |  |  |  |  |

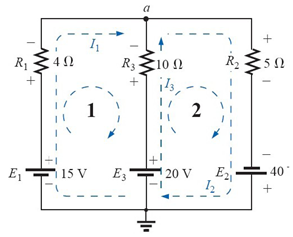
**INFERENCE**

**T**he Kirchoff’s Voltage Law (KVL) for the given circuit is verified.

**REVIEW QUESTIONS**

1. 1. Verify KCL and KVL for the given circuit.
2. 2. Comment on the inferences .

3.Find I1 , I2 , I3 .



|  |  |
| --- | --- |
| **EXP NO: 9** | **VERIFICATION OF THEVENIN’S & NORTON’S THEOREM** |
| **DATE:** |

**(a)VERIFICATION OF THEVENIN’S THEOREM**

**AIM**

To verify Thevenin’s theorem and to find the current flowing through the load resistance.

**COMPONENTS/EQUIPMENTS REQUIRED**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **S.NO** | **COMPONENTS/EQUIPMENTS** | **TYPE** | **RANGE** | **QUANTITY** |
| 1 | Regulated Power Supply | DC | (0-30)V | 1 |
| 2 | Resistor | - | 1KΩ | 3 |
| 3 | Ammeter | DC | (0-10)mA | 1 |
| 4 | Bread board | - | - | 1 |
| 5 | Connecting wires | - | - | Few |

**THEORY**

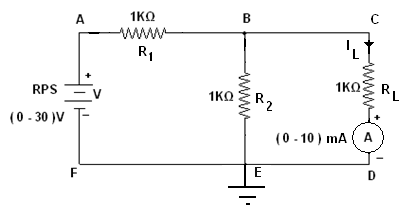
**THEVENIN’S THEOREM**

Any linear active network with output terminals C and D can be replaced by a single voltage source (VTh = VOc) in series with a single impedance (ZTh = Zi).

VTh is the Thevenin’s voltage. It is the voltage between the terminals C and D on open circuit condition. Hence it is called open circuit voltage denoted by VOc.

ZTh is called Thevenin’s impedance. It is the driving point impedance at the terminals C and D when all the internal sources are set to zero. In case of DC ZTh is replaced by RTh.

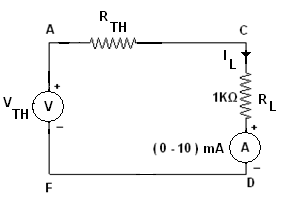
**CIRCUIT DIAGRAM**

****

**Circuit Diagram for Thevenin’s Theorem**

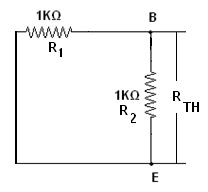
**THEORETICAL CALCULATION:**

The Thevenin’s equivalent circuit is,





**To Find RTH:**

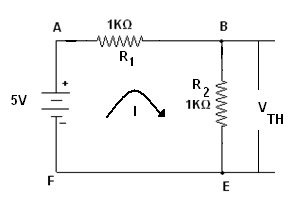


= 1K = 1K ;

RTH= R1\*R2 =0.5KΩ

R1+R2

**To Find VTH:**





=2.5mA

VTH=I\*R2=2.5V

**Let V = 5V,**

VTH=VBE

=

=2.5/(1.5KΩ)=1.67mA

**PROCEDURE:**

1. The circuit connections are given as per the circuit diagram.
2. Switch ON the power supply.
3. Initially set 5V as input voltage from RPS.
4. The ammeter reading is noted and the value is tabulated.

**TABULATION:**

**Let V = 5V**

|  |  |  |  |
| --- | --- | --- | --- |
| **S.No** | **Voltage in Volts** | **Load Current in Amps** | |
| **Theoretical Value** | **Practical Value** |
| 1 | 5 | 1.67mA |  |

**INFERENCE**

The Thevenin’s theorem was verified for the given circuit.

**Theoretical: Practical:**

Vth = 2.5V Vth =

Rth =0.5KΩ Rth =

IL = 1.67mA IL =

**(b) VERIFICATION OF NORTON’S THEOREM**

**AIM**

To verify Norton’s theorem and to determine the current flow through the load resistance.

**COMPONENTS/EQUIPMENTS REQUIRED**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **S.NO** | **COMPONENTS/EQUIPMENTS** | **TYPE** | **RANGE** | **QUANTITY** |
| 1 | Regulated Power Supply | DC | (0-30)V | 1 |
| 2 | Resistor | - | 1KΩ | 3 |
| 3 | Ammeter | DC | (0-10)mA | 1 |
| 4 | Bread board | - | - | 1 |
| 5 | Connecting wires | - | - | Few |

**THEORY:**

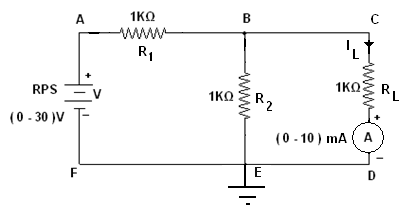
**NORTON’S THEOREM:**

Any linear active network with output terminals C and D can be replaced by a single current source ISC(IN) in parallel with a single impedance (ZTh = Zn).

ISC is the current through the terminals C and D on short circuit condition. ZTh is called Thevenin’s impedance. In case of DC ZTh is replaced by RTh.

The current through impedance connected to the terminals of the Norton’s equivalent circuit must have the same direction as the current through the same impedance connected to the original active network.

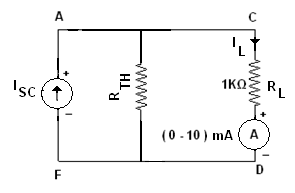
**CIRCUIT DIAGRAM**

****

**Circuit Diagram for Norton’s Theorem**

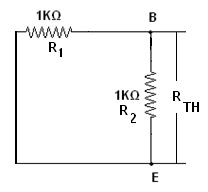
**THEORETICAL CALCULATION:**

The Norton’s equivalent circuit is,

****



**To Find RTH:**



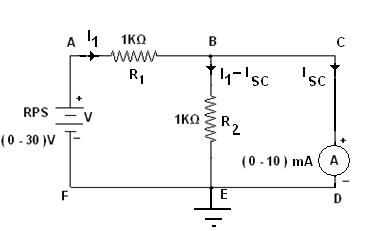
= 1K = 1K ;

RTH= R1\*R2

R1+R2

=0.5KΩ

**To Find ISC:**



**Let V=5V**

In the loop ABEFA by applying KVL,







In the loop BCDEB by applying KVL,







From the equation (I) and (2),



∴

IL = ISC\*RTH

RTH+RL

=1.67mA

**PROCEDURE:**

1. The circuit connections are given as per the circuit diagram.
2. Switch ON the power supply.
3. Initially set 5V as input voltage from RPS.
4. The ammeter reading is noted and the value is tabulated.

**TABULATION:**

**Let V = 5V**

|  |  |  |
| --- | --- | --- |
|  | **ISC** | **IL** |
| Theoritical | 5mA | 1.67mA |
| Practical |  |  |

**INFERENCE**

The Norton’s theorem was verified for the given circuit.

**Theoretical:**  **Practical:**

Isc = 5mA Isc =

Rth =0.5KΩ Rth =

IL = 1.67mA IL =

|  |  |
| --- | --- |
| **EXP NO: 10** | **VERIFICATION OF SUPERPOSITION THEOREM** |
| **DATE:** |

**AIM**

To verify superposition theorem and determine the current following through the load resistance.

**COMPONENTS/EQUIPMENTS REQUIRED**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **S.NO** | **COMPONENTS/EQUIPMENTS** | **TYPE** | **RANGE** | **QUANTITY** |
| 1 | Regulated Power Supply | DC | (0-30)V | 2 |
| 2 | Resistor | - | 1KΩ | 3 |
| 3 | Ammeter | DC | (0-10)mA | 1 |
| 4 | Bread board | - | - | 1 |
| 5 | Connecting wires | - | - | Few |

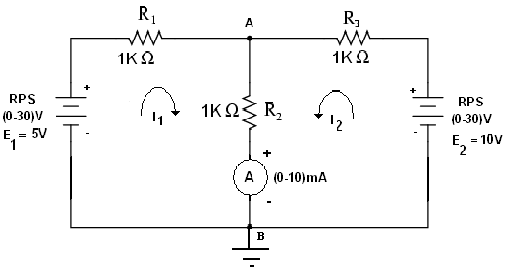
**THEORY:**

**SUPERPOSITION THEOREM:**

The superposition theorem for [electrical circuits](http://en.wikipedia.org/wiki/Electrical_network) states that the total [current](http://en.wikipedia.org/wiki/Electric_current) in any branch of a bilateral linear circuit equals the algebraic sum of the currents produced by each source acting separately throughout the circuit.To ascertain the contribution of each individual source, all of the other sources first must be "killed" (set to zero) by:

1. replacing all other [voltage sources](http://en.wikipedia.org/wiki/Voltage_source) with a [short circuit](http://en.wikipedia.org/wiki/Short_circuit) (thereby eliminating difference of potential. i.e. V=0)
2. replacing all other [current sources](http://en.wikipedia.org/wiki/Current_source) with an [open circuit](http://en.wikipedia.org/wiki/Open_circuit) (thereby eliminating current. i.e. I=0)
3. This procedure is followed for each source in turn, and then the resultant currents are added to determine the true operation of the circuit. The resultant circuit operation is the superposition of the various voltage and current sources.

**CIRCUIT DIAGRAM**

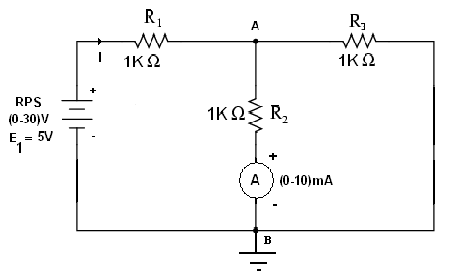


**Circuit Diagram for Superposition Theorem**

**TABULATION:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| S.No | E**1** voltage(Volts) | E**2** voltage(Volts) | Load current across the branch AB (mA) | |
| Theoritical | Practical |
| 1 | 5V | 10V | 4.95mA |  |

**E1 SOURCE IS ACTING:**



**THEORETICAL CALCULATION:**

= 1K = 1K ; = 1K





=1.5KΩ



=3.3mA

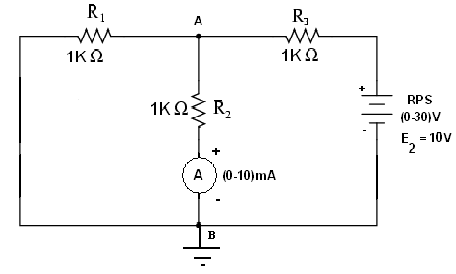
Let V = 5V,

 =1.65mA

**TABULATION:**

|  |  |  |  |
| --- | --- | --- | --- |
| S.No | E**1** voltage(Volts) | Load current across the branch AB (mA) | |
| Theoritical | Practical |
| 1 | 5 | 1.65mA |  |

**E2 SOURCE IS ACTING:**



**THEORETICAL CALCULATION:**

= 1K = 1K ; = 1K





=1.5KΩ



=6.67mA

Let V = 10V,

=3.3mA

**TABULATION:**

|  |  |  |  |
| --- | --- | --- | --- |
| S.No | E**2** voltage(Volts) | Load current across the branch AB (mA) | |
| Theoritical | Practical |
| 1 | 10 | 3.3mA |  |

**E1 and E2 SOURCES ARE ACTING:**

=5mA

**INFERENCE**

**T**he superposition theorem for the given circuit is verified.

|  |  |
| --- | --- |
| **EXP NO: 11** | **VERIFICATION OF MAXIMUM POWER TRANSFER & RECIPROCITY THEOREM** |
| **DATE:** |

**(a)VERIFICATION OF MAXIMUM POWER TRANSFER THEOREM**

**AIM**

To find the value of resistance RL in which maximum power is transferred to the load resistance.

**COMPONENTS/EQUIPMENTS REQUIRED**

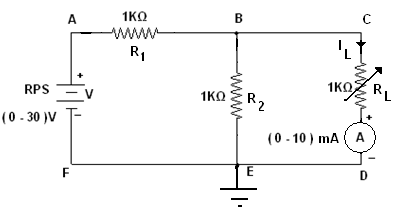
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **S.NO** | **COMPONENTS/EQUIPMENTS** | **TYPE** | **RANGE** | **QUANTITY** |
| 1 | Regulated Power Supply | DC | (0-30)V | 1 |
| 2 | Resistor | - | 1KΩ | 2 |
| 3 | Variable Resistor |  | 1KΩ | 1 |
| 4 | Ammeter | DC | (0-10)mA | 1 |
| 5 | Bread board | - | - | 1 |
| 6 | Connecting wires | - | - | Few |

**THEORY:**

**MAXIMUM POWER TRANSFER THEOREM:**

In electrical engineering, the **maximum power (transfer) theorem** states that, to obtain maximum external power from a source to a load with a finite internal resistance, the resistance of the load must be made the same as that of the source. The theorem applies to maximum power, and not maximum efficiency. If the resistance of the load is made larger than the resistance of the source, then efficiency is higher, since most of the power is generated in the load, but the overall power is lower since the total circuit resistance goes up. If the internal impedance is made larger than the load then most of the power ends up being dissipated in the source, and although the total power dissipated is higher, due to a lower circuit resistance, it turns out that the amount dissipated in the load is reduced.

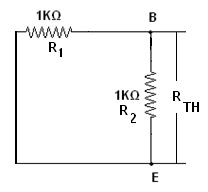
**CIRCUIT DIAGRAM**

****

**Circuit Diagram for Maximum Power TransferTheorem**

**THEORETICAL CALCULATION:**

**To Find RTH:**

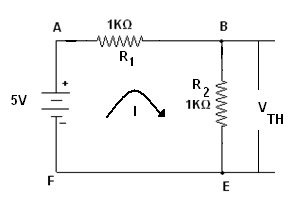


= 1K = 1K ;



=0.5KΩ

**To Find VTH:**





=2.5mA

VTH=R2\*I=2.5V

**Let V = 5V,**







Load Resistance RL=Rth=0.5KΩ

**PROCEDURE:**

1. The circuit connections are given as per the circuit diagram.
2. Switch ON the power supply.
3. Initially set 5V as input voltage from RPS.
4. The ammeter reading is noted for various values of load resistance and the values are tabulated.
5. The load resistance for the maximum power is obtained from the table.

**TABULATION:**

**Let V = 5V**

|  |  |  |  |
| --- | --- | --- | --- |
| S.No | **Resistance(RL) in Ohms** | **Current(IL)**  **in mA** | **Power (IL2RL)**  **in mW** |
| 1 | 100 |  |  |
| 2 | 200 |  |  |
| 3 | 300 |  |  |
| 4 | 400 |  |  |
| 5 | 500 |  |  |
| 6 | 700 |  |  |
| 7 | 900 |  |  |

**INFERENCE :**

**T**he value of unknown resistance in which the maximum power is transferred to the load was found. Theoretical load resistance = 0.5KΩ

Practical load resistance =0.5KΩ Maximum power = 2.53mA

**(b)VERIFICATION OF RECIPROCITY THEOREM**

**AIM**

To verify Reciprocity theorem and to determine the current flow through the load resistance.**COMPONENTS/EQUIPMENTS REQUIRED**

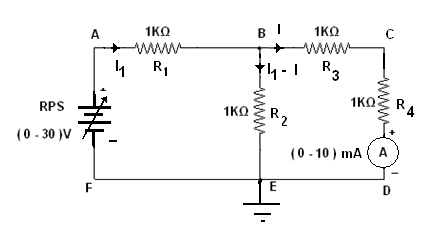
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **S.NO** | **COMPONENTS/EQUIPMENTS** | **TYPE** | **RANGE** | **QUANTITY** |
| 1 | Regulated Power Supply | DC | (0-30)V | 1 |
| 2 | Resistor | - | 1KΩ | 4 |
| 3 | Ammeter | DC | (0-5)mA | 1 |
| 4 | Bread board | - | - | 1 |
| 5 | Connecting wires | - | - | Few |

**THEORY:**

**RECIPROCITY THEOREM:**

The reciprocity theorem states that if an emf ‘E’ in one branch of a reciprocal network produces a current I in another, then if the emf ‘E’ is moved from the first to the second branch, it will cause the same current in the first branch, where the emf has been replaced by a short circuit. We shall see that any network composed of linear, bilateral elements (such as R, L and C) is reciprocal.

**BEFORE INTERCHANGING**

****

**Circuit Diagram for ReciprocityTheorem**

**THEORETICAL CALCULATION:**

**Let V=5V**

In the loop ABEF by applying KVL,







In the loop BCDE by applying KVL,







D = 





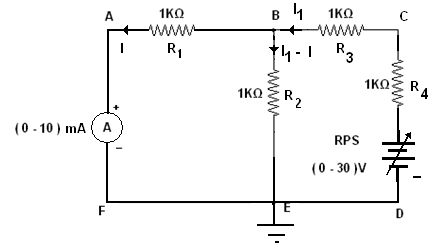
**PROCEDURE:**

1. The circuit connections are given as per the circuit diagram.
2. Switch ON the power supply.
3. Initially set 5V as input voltage from RPS.
4. The ammeter reading is noted and tabulated.

**TABLEFOR BEFORE INTERCHANGING:**

|  |  |  |
| --- | --- | --- |
| **V (Volts)** | **Current (mA)** | |
| Theoritical | Practical |
| 5 | 1 |  |

**AFTER INTERCHANGING:**

****

**Circuit Diagram for ReciprocityTheorem**

**THEORETICAL CALCULATION:**

Let V=5V.

In the loop ABEFA by applying KVL,







In the loop BCDE B by applying KVL,







D = 





**PROCEDURE:**

1. The circuit connections are given as per the circuit diagram.
2. Switch ON the power supply.
3. Initially set 5V as input voltage from RPS.
4. The ammeter reading is noted and tabulated.

**TABLEFOR AFTER INTERCHANGING:**

|  |  |  |
| --- | --- | --- |
| **V (Volts)** | **Current (mA)** | |
| Theoritical | Practical |
| 5 | 1 |  |

**INFERENCE :**

**T**he reciprocity theorem for the given circuit is verified.

|  |  |
| --- | --- |
| **EXP NO: 12** | **FREQUENCY RESPONSE OF SERIES AND PARALLEL RESONANCE CIRCUIT** |
| **DATE:** |

**AIM**

To analyze the frequency response of series and parallel resonance circuits.

**COMPONENTS/EQUIPMENTS REQUIRED**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **S.NO** | **COMPONENTS/EQUIPMENTS** | **TYPE** | **RANGE** | **QUANTITY** |
| 1 | Function Generator | AC | (1Hz-3MHz) | 1 |
| 2 | Resistor | AC | 600Ω | 1 |
| 3 | Inductor | AC | 101.4mH | 1 |
| 4 | Capacitor | AC | 0.01mF | 1 |
| 5 | Ammeter | AC | (0-10)mA | 1 |
| 6 | Bread board | - | - | 1 |
| 7 | Connecting wires | - | - | Few |

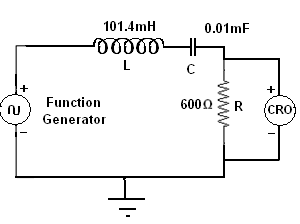
**THEORY:**

The resonance of a RLC circuit occurs when the inductive and capacitive reactance are equal in magnitude but cancel each other because they are 180 degrees apart in phase. The sharp minimum in impedance which occurs is useful in tuning applications. The sharpness of the minimum depends on the value of R.

The frequency at which the reactance of the inductance and the capacitance cancel each other is the resonant frequency (or the unity power factor frequency) of this circuit. This occurs at



**SERIES RESONANCE:**

****

**Circuit Diagram for Series Resonant**

**THEORETICAL CALCULATION:**

R = 560Ω

L = 101mH

C = 0.01µF



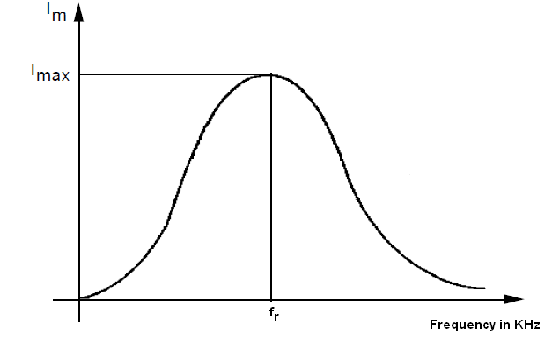


**PROCEDURE:**

1. The circuit connections are given as per the circuit diagram.
2. Switch ON the power supply.
3. The input is given in the form of sin wave by function generator.
4. The amplitude of the response across the resistor is noted for various frequency ranges.
5. The current is calculated and tabulated.

**TABULATION:**

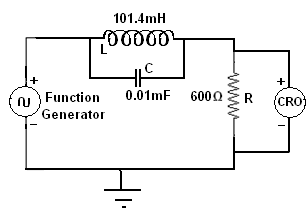
|  |  |  |  |
| --- | --- | --- | --- |
| **S.No** | **Frequncy (KHz)** | **Output voltage (mVolts)** | **I = V / R**  **(mA)** |
| **1** | **1** |  |  |
| **2** | **2** |  |  |
| **3** | **3** |  |  |
| **4** | **4** |  |  |
| **5** | **4.5** |  |  |
| **6** | **5** |  |  |
| **7** | **6** |  |  |
| **8** | **7** |  |  |



**Frequency Response of Series Resonance Circuit**

**PARALLEL RESONANCE:**

|  |
| --- |
|  |

****

**Circuit Diagram for Parallel Resonant**

**THEORETICAL CALCULATION:**

R = 560Ω

L = 101.4mH

C = 0.01µF





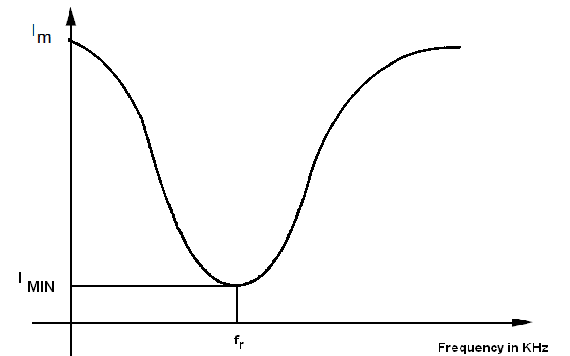
**PROCEDURE:**

1. The circuit connections are given as per the circuit diagram.
2. Switch ON the power supply.
3. The input is given in the form of sin wave by function generator.
4. The amplitude of the response across the resistor is noted for various frequency ranges.
5. The current is calculated and tabulated.

**TABULATION:**

|  |  |  |  |
| --- | --- | --- | --- |
| **S.No** | **Frequency (KHz)** | **Output voltage (Volts)** | **I = V / R**  **(mA)** |
| **1** | **1** |  |  |
| **2** | **2** |  |  |
| **3** | **3** |  |  |
| **4** | **4** |  |  |
| **5** | **4.5** |  |  |
| **6** | **5** |  |  |
| **7** | **6** |  |  |
| **8** | **7** |  |  |

**MODEL GRAPH:**

****

**Frequency Response of Parallel Resonance Circuit**

**INFERENCE :**

**T**he frequency response of series and parallel resonant circuits are analyzed.

|  |  |
| --- | --- |
| **EXP NO: 13** | **TRANSIENT ANALYSIS OF RL AND RC CIRCUITS** |
| **DATE:** |

**AIM**

To construct RL & RC transient circuit and to study the transient curves.

**COMPONENTS/EQUIPMENTS REQUIRED**

|  |  |  |  |
| --- | --- | --- | --- |
| **S. NO.** | **COMPONENTS/EQUIPMENTS** | **RANGE** | **QUANTITY** |
|  | Resistor | 10kΩ | 3 |
|  | Ammeter | (0-10)mA | 1 |
|  | Voltmeter | (0-10)V | 1 |
|  | Capacitor | 1000µF | 1 |
|  | Regulated Power Supply | (0-30)V | 1 |
|  | Bread Board |  | 1 |
|  | Connecting Wires |  | As required |

KNOWLEDGE REQUIRED

Transient analysis & passive components.

FORMULA USED

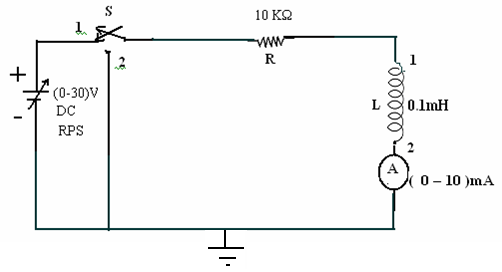
Time constant of RC circuit = RC

PROCEDURE

1. Connections are made as per the circuit diagram.
2. Before switching ON the power supply the switch S should be in off position
3. Now switch ON the power supply and change the switch to ON position.
4. The voltage is gradually increased and note down the reading of ammeter and voltmeter for
5. each time duration in RC.In RL circuit measure the Ammeter reading.
6. Tabulate the readings and draw the graph of Vc(t)Vs t

**CIRCUIT DIAGRAM**

**RL CIRCUIT**

****

**MODEL GRAPH**

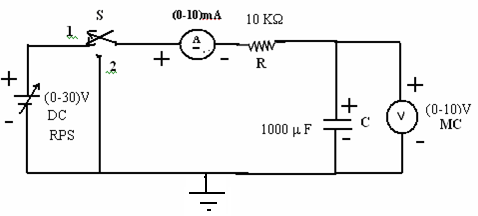
****

**TABULATION**

|  |  |  |  |
| --- | --- | --- | --- |
| **S.No.** | **TIME (msec)** | **CHARGING CURRENT (I) A** | **DISCHARGING CURRENT (I) A** |
|  |  |  |  |

**CIRCUIT DIAGRAM**

**RC CIRCUIT**

****

**MODEL GRAPH**

**CHARGING DISCHARGING**

****

**TABULATION**

|  |  |  |  |
| --- | --- | --- | --- |
|  | **TIME (msec)** | **VOLTAGE ACROSS ‘C’**  **(volts)** | **CURRENT THROUGH ‘C’**  **(mA)** |
| Charging |  |  |  |
| Discharging |  |  |  |

**INFERENCE :**

The transient response of the given RL & RC circuits were analyzed.

ADDITIONAL EXPERIMENTS

|  |  |
| --- | --- |
| **EXP NO:** | **CHARACTERISTICS OF DIAC** |
| **DATE:** |

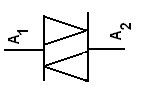
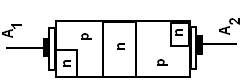
**AIM**

To study and plot the V-I characteristics of a DIAC.

**COMPONENTS & EQUIPMENTS REQUIRED:**

|  |  |  |  |
| --- | --- | --- | --- |
| **S.NO** | **COMPONENTS & EQUIPMENTS** | **TYPE** | **QUANTITY** |
| 1 | Regulated Power Supply | (0-30)V | 1 |
| 2 | Resistor | 1KΩ | 1 |
| 3 | DC Voltmeter | (0-30)V | 1 |
| 5 | DC Ammeter | (0-30)mA | 1 |
| 6 | DIAC |  | 1 |
| 7 | Bread board | - | 1 |
| 8 | Connecting wires | - | Few |

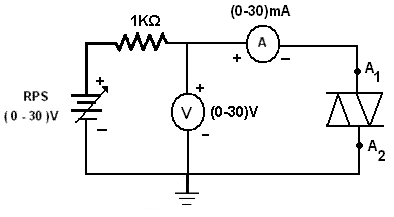
**THEORY:**



**Construction Symbol**

The DIAC is basically two parallel diodes turned in opposite direction having a pair of four layer diodes for alternating current. It is a bidirectional trigger diode that conducts current only after its breakdown voltage has been exceeded momentarily. When this occurs, the resistance of the diode abruptly decreases, leading to a sharp decrease in the voltage drop across the diode and, usually, a sharp increase in current flow through the diode. The diode remains "in conduction" until the current flow through it drops below a value characteristic for the device, called the holding current. Below this value, the diode switches back to its high-resistance (non-conducting) state. When used in AC applications this automatically happens when the current reverses polarity.

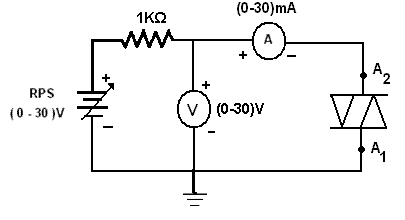
**FORWARD BIAS:**

****

**PROCEDURE:**

1. Connections are given as per the circuit diagram.
2. The supply is switched ON.
3. Vary the power supply in regular step and note down the voltage and current of DIAC.
4. Plot the graph between the voltage and current.

**REVERSE BIAS:**

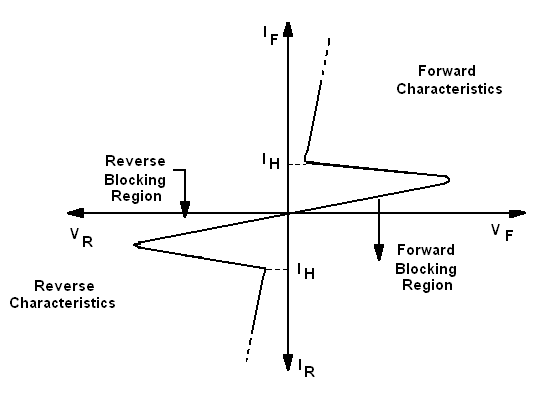
****

**PROCEDURE:**

1. Connections are given as per the circuit diagram.
2. The supply is switched ON.
3. Vary the power supply in regular step and note down the voltage and current of DIAC.
4. Plot the graph between the voltage and current.

**TABULATION**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **S.No** | **FORWARD BIAS** | | **REVERSE BIAS** | |
| **Voltage(V)** | **Current(mA)** | **Voltage(V)** | **Current(mA)** |
| **1** |  |  |  |  |
| **2** |  |  |  |  |
| **3** |  |  |  |  |
| **4** |  |  |  |  |
| **5** |  |  |  |  |
| **6** |  |  |  |  |
| **7** |  |  |  |  |
| **8** |  |  |  |  |
| **9** |  |  |  |  |
| **10** |  |  |  |  |

****

**V-I characteristics of a DIAC**

**INFERENCE**

The V-I characteristics of a DIAC is analyzed and the plotted.

|  |  |
| --- | --- |
| **EXP NO:** | **CHARACTERISTICS OF TRIAC** |
| **DATE:** |

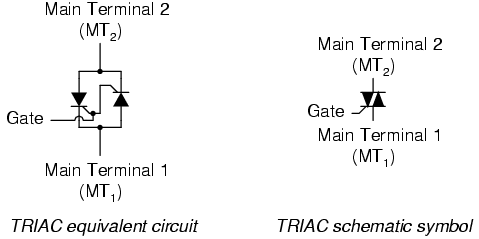
**AIM**

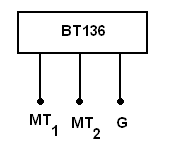
To study and plot the V-I characteristics of a TRIAC.

**COMPONENTS & EQUIPMENTS REQUIRED:**

|  |  |  |  |
| --- | --- | --- | --- |
| **S.NO** | **COMPONENTS /EQUIPMENTS** | **TYPE** | **QUANTITY** |
| 1 | Regulated Power Supply | (0-30)V | 2 |
| 2 | Resistor | 10 KΩ,5 KΩ | 1,1 |
| 3 | DC Voltmeter | (0-30)V | 1 |
| 5 | DC Ammeter | (0-100)mA | 2 |
| 6 | TRIAC | BT136 | 1 |
| 7 | Bread board | - | 1 |
| 8 | Connecting wires | - | Few |

**THEORY:**

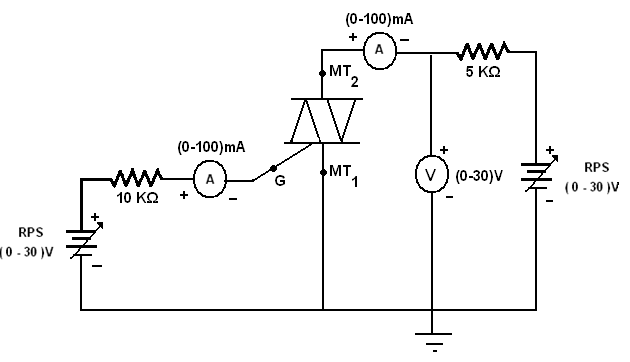




**Pin Diagram**

It is basically two SCR’s turned in opposite directions, with a common gate terminal. It is a bidirectional device. The two main electrodes are called MT1 and MT2 while common control terminal is called gate G. S The gate terminal is near to MT1. The triac can be turned ON by applying either positive or negative voltage to the gate G with respect to the main terminal MT1.

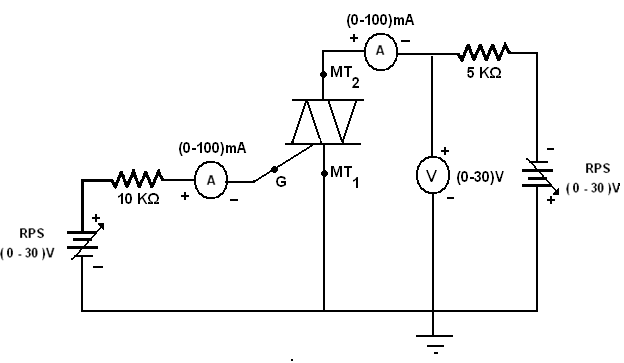
**FORWARD BIAS:**

****

**PROCEDURE:**

1. Connections are given as per the circuit diagram.
2. The supply is switched ON.
3. The Gate current IG is set to 2mA by varying the RPS which connected to the gate.
4. Vary another power supply which is connected across the terminals of TRIAC in regular step and note down the voltage and current of TRIAC.
5. Plot the graph between the voltage and current.

**REVERSE BIAS:**

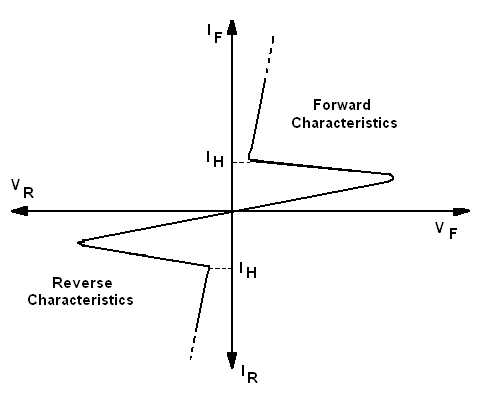
****

**PROCEDURE:**

1. Connections are given as per the circuit diagram.
2. The supply is switched ON.
3. The Gate current IG is set to 2mA by varying the RPS which connected to the gate.
4. Vary another power supply which is connected across the terminals of TRIAC in regular step and note down the voltage and current of TRIAC.
5. Plot the graph between the voltage and current.

**TABLE**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **S.No** | **FORWARD BIAS** | | **REVERSE BIAS** | |
| **Gate Current (IG= 2mA)** | | **Gate Current (IG= 2mA)** | |
| **Voltage(V)** | **Current(mA)** | **Voltage(V)** | **Current(mA)** |
| **1** |  |  |  |  |
| **2** |  |  |  |  |
| **3** |  |  |  |  |
| **4** |  |  |  |  |
| **5** |  |  |  |  |
| **6** |  |  |  |  |
| **7** |  |  |  |  |
| **8** |  |  |  |  |
| **9** |  |  |  |  |

****

**V-I characteristics of a TRIAC**

**INFERENCE**

The V-I characteristics of a DIAC is analyzed and the plotted.

|  |  |
| --- | --- |
| **EXP NO:** | **CHARACTERISTICS OF UJT** |
| **DATE:** |

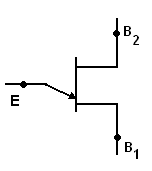
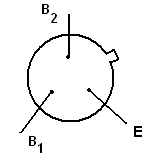
**AIM:**

To study and plot the characteristics of uni junction transistor (UJT) and to determine the peak voltage (VP), valley point voltage (VV), valley point current (IV) and intrinsic standoff ratio (η).

**COMPONENTS & EQUIPMENTS REQUIRED:**

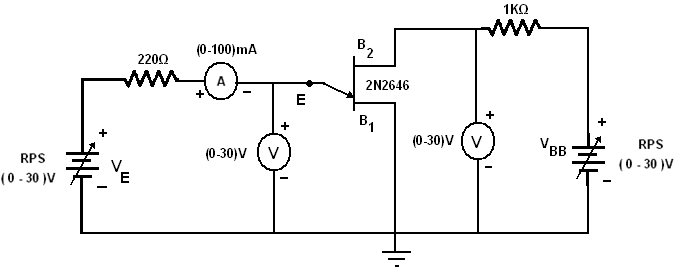
|  |  |  |  |
| --- | --- | --- | --- |
| **S.NO** | **COMPONENTS & EQUIPMENTS** | **RANGE** | **QUANTITY** |
| 1 | Regulated Power Supply | (0-30)V | 2 |
| 2 | Resistor | 1KΩ | 1 |
| 3 | Resistor | 220Ω | 1 |
| 3 | DC Voltmeter | (0-30)V | 2 |
| 5 | DC Ammeter | (0-100)mA | 1 |
| 6 | UJT | 2N2646 | 1 |
| 7 | Bread board | - | 1 |
| 8 | Connecting wires | - | Few |

**THEORY:**



**Pin Diagram of UJT Symbol of UJT**

The UJT is essentially a bar of N type semiconductor material into which P type material has been diffused somewhere along its length.

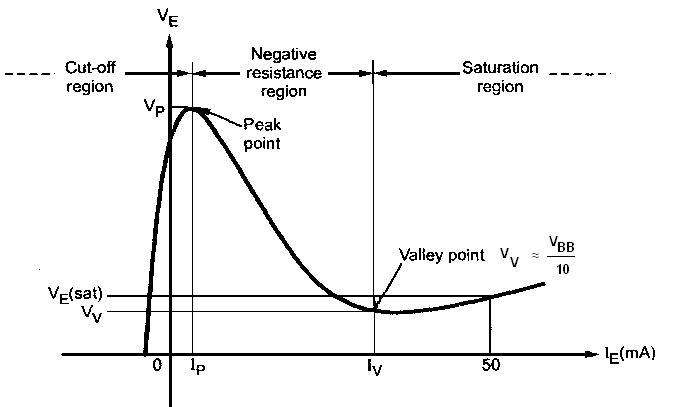


**PROCEDURE:**

1. Connections are given as per the circuit diagram.
2. The supply is switched ON.
3. Set the voltage across base 1 and base 2 (VBB) is constant.
4. Vary the voltage across emitter and base 1 (VE) and note down the emitter current (IE).
5. Repeat the above procedure for various VBB.
6. Plot the graph between VE and IE.
7. From the plot determine the

**TABLE**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **S.No** | **VBB­= 5V** | | **VBB­= 5V** | |
| **VE(volts)** | **IE (mA)** | **VE(volts)** | **IE (mA)** |
| 1 |  |  |  |  |
| 2 |  |  |  |  |
| 3 |  |  |  |  |
| 4 |  |  |  |  |
| 5 |  |  |  |  |
| 6 |  |  |  |  |
| 7 |  |  |  |  |
| 8 |  |  |  |  |
| 9 |  |  |  |  |



**Characteristics of a UJT**

The characteristics can be divided into three main regions which are,

1. **Cut-off region**: The emitter voltage VE is less than VP and the p-n junction is reverse biased. A small amount of reverse saturation current flows through the device, which is negligibly small of the order of µA. This condition remains till the peak point.
2. **Negative resistance region:** When the emitter voltage VE becomes equal to VP the p-n junction becomes forward biased and IE starts flowing. The voltage across the device decreases in this region, though the current through the device increases. Hence the region is called negative resistance region. This region continues till valley point.
3. **Saturation region:** Increase in IE further valley point current IV drives the device in the saturation region. The voltage corresponding to valley point is called valley point voltage denoted as VV In this region, further decrease in voltage does not take place. The characteristic is similar to that of a semiconductor diode, in this region.

From the plot,

1. VP =
2. VV =
3. IV =
4. η = **Error! Reference source not found.**(VP – VD) / VBB =

Where VD = The diode drop

= 0.3 to 0.7 V

**INFERENCE**

Thus the characteristic of a Uni Junction Transistor(UJT) is analyzed and the peak voltage (VP), valley point voltage (VV), valley point current (IV) and intrinsic standoff ratio (η) are determined.

|  |  |
| --- | --- |
| **EXP NO:** | **CHARACTERISTICS OF PHOTO DIODE** |
| **DATE:** |

**AIM:**

To study and plot the characteristics of a Photo Diode.

**COMPONENTS & EQUIPMENTS REQUIRED:**

|  |  |  |  |
| --- | --- | --- | --- |
| **S.NO** | **COMPONENTS & EQUIPMENTS** | **RANGE** | **QUANTITY** |
| 1 | Regulated Power Supply | (0-30)V | 1 |
| 2 | Resistor | 1KΩ | 1 |
| 3 | DC Voltmeter | (0-30)V | 1 |
| 4 | DC Ammeter | (0-50)mA | 1 |
| 5 | Photo Diode |  | 1 |
| 6 | Bread board | - | 1 |
| 7 | Connecting wires | - | Few |

**THEORY:**



**Symbol**

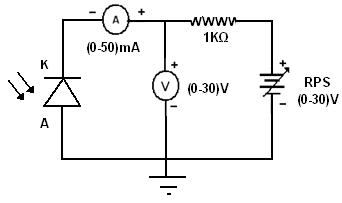
The photodiode is a semiconductor p-n junction device whose region of operation is limited to the reverse biased region.

The reverse current without light in diode is in the range of µA. The change in this current due to the light is also in the range of µA. Thus such a change can be significantly observed in the reverse current. If the photodiode is forward biased, the current flowing through it is in mA. The applied forward biased voltage takes the control of the current instead of the light. The change in forward current due to light is negligible and cannot be noticed. The resistance of forward biased diode is not affected by the light. Hence to have significant effect of light on the current and to operate photodiode as a variable resistance device, it is always connected in reverse biased condition.

The depletion region width is large. Under normal condition, it carries small reverse current due to minority charge carriers. When light is incident through glass window on the p-n junction, photons in the light bombarding the p-n junction and some energy is imparted to the valence electrons. Due to this, valence electrons are dislodged from the covalent bonds and become free electrons. Thus more electron-hole pairs are generated. Thus total number of minority charge carriers increases and hence the reverse current increases.

When there is no light, the reverse biased photodiode carries a current which is very small and called **dark current**. It is purely due to thermally generated minority carriers. When light is allowed to fall on a p-n junction through a small window, photons transfer energy to valence electrons to make them free. Hence reverse current increases. It is proportional to the light intensity. The reverse current is not dependent on reverse voltage and totally depends on light intensity.

**CIRCUIT DIAGRAM**

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**PROCEDURE:**

1. Connections are given as per the circuit diagram.

2. Connect the patch card from one of the devices mounted in the moving plot to the main unit.

3. Connect the unit to the 220V supply. Switch ON the toggle switch. LED will glow that indicating that the unit is ready for operation.

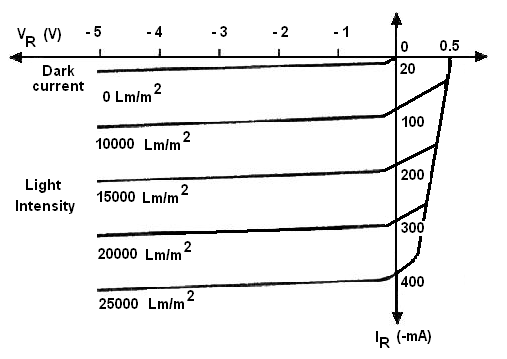
4. Connect the mains card of the light source to 220V AC supply and switch ON the controller.

5. Adjust the distance between the light source and photo diode. Note down the current and voltage for various distances.

6. Plot the graph between the reverse voltage and reverse current.

**TABLE**

|  |  |  |  |
| --- | --- | --- | --- |
| **S.No** | **Distance(mm)** | **Voltage(V)** | **Current(mA)** |
| **1** |  |  |  |
| **2** |  |  |  |
| **3** |  |  |  |
| **4** |  |  |  |
| **5** |  |  |  |
| **6** |  |  |  |
| **7** |  |  |  |

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**Photo Diode Characteristics**

**INFERENCE**

The characteristic of a photo diode is analyzed.